MONTEK SINGH

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PERSONAL INFORMATION

Research Interests

Design and test of asynchronous circuits and systems
CAD tools for asynchronous design
Heterogeneous mixed-timing systems
Power-aware graphics hardware
Hardware security and authentication

Education

Columbia University, New York, NY	Computer Science	Ph.D., February 2002
Columbia University, New York, NY	Computer Science	M.S., October 1996
Indian Institute of Technology, Delhi, India	Electrical Engineering	B.Tech, May 1993

Professional Experience

2001-present	Assistant Professor, Dept. of Computer Science, Univ. of North Carolina at Chapel Hill
2007-present	Ad-hoc Faculty Member, ECE Dept., Duke University, Durham, NC
1994-2001	Graduate Research Assistant, Dept. of Computer Science, Columbia University, NY
2000 Fall	Research Intern, IBM T.J. Watson Research Center, Yorktown Heights, NY
1999 Summer	Academic Visitor, Amulet Group, University of Manchester, Manchester, UK
1997 Summer	Summer Intern, Intel Corp., Santa Clara, CA
1992 Summer	Practical Trainee, Bhabha Atomic Research Center, Bombay, India

RECENT AWARDS AND HONORS

- **Best Paper Award,** 6th IEEE ASYNC Symposium, Eilat, Israel, April 2000.
  (International Symposium on Asynchronous Circuits and Systems)

- **Best Paper Finalist,** 8th IEEE ASYNC Symposium, Manchester, UK, April 2002.
  (International Symposium on Asynchronous Circuits and Systems)

- UNC Junior Faculty Development Award, December 2002.

- IBM Faculty Award, August 2004.

RESEARCH SUPPORT

External Funding

- NSF (pending): *"Power-Aware Graphics Hardware,"* co-PI (PI: Prof. Anselmo Lastra). Submitted October 2006, $500K.

- NSF (pending): *"CAREER: Design and Test of Novel Asynchronous High-Speed VLSI Architectures for Stream Processing,"* PI. Submitted July 2006, $570K.

- DARPA (pending): *"TRUSTed Hardware Authentication,"* co-PI (PI: Dr. Warren Snapp, Boeing Inc.). Submitted August 2006. UNC share: $300K; total $15M.

  I was invited by Boeing to be a part of the team (consisting of two major companies and four universities) that has proposed a major research effort in hardware security and authentication. The objective is to detect malicious modifications to microelectronic chips. My work in on the key aspect of timing fingerprint generation and timing-fingerprint-based authentication.

- DARPA: *"High-Speed Clockless Pipeline Design Flow,"* PI (subcontract via Boeing), under the CLASS program ("Clockless Logic Analysis, Synthesis, and Systems"), March 2005-present. UNC share: $275K; total $14M.

  I am part of a multi-group team, led by Boeing, which has been awarded the largest grant in asynchronous design in the U.S. in over 20 years. There were over twenty proposals, and only one team was awarded. I was invited to the join the program for Phases 2 and 3 in order to fill a critical need. I am playing the crucial role of develop an automated high-speed pipeline synthesis flow, building upon my research in high-speed asynchronous pipeline circuits. My task has become the single high-speed design option for the entire program. In collaboration with Handshake Solutions (a Philips spin-off), we have successfully developed a new experimental high-speed pipeline design flow based on their Haste flow.

  Follow-Up DARPA Funding (pending): I was invited by Boeing to be part of the team that is aiming for a follow-up contract. Discussions are currently underway between Boeing and DARPA. My role will be on further development and optimization of the high-speed pipeline synthesis flow, including system-level performance analysis and optimization tools, and on test and design-for-testability.

- IBM: *"Design of Latency-Insensitive Systems,"* PI (IBM Faculty Award), August 2004-July 2005. $20K

Internal Funding

- UNC: Junior Faculty Development Award, December 2002, $5,000.

- UNC: University Research Council Research Grant, December 2002, $2,300.

Funding Awards for My Students

- NSF Graduate Fellowship: Gennette Gill, Mar 2004. Approx. $40K/year for 3 years = $120K.
- Dept. of Defense Graduate Fellowship (NDSEG): Gennette Gill, April 2004. Approx. $40K/year for 3 years = $120K.
- ATI Graduate Fellowship: Justin Hensley, May 2004. Approx. $35/year for 2 years = $70K.
- NSF East-Asia Summer Fellowship: Todd Gamblin, Feb 2004. Approx. $10K.

PATENTS ISSUED

- Circuits and methods for high-capacity asynchronous pipeline processing, US Patent 7,053,665 granted May 30, 2006.
- Asynchronous pipeline with latch controllers, US Patent 6,958,627 granted October 25, 2005.
- Circuits and methods for high-capacity asynchronous pipeline, US Patent 6,867,620 granted March 15, 2005.
- High-throughput asynchronous dynamic pipelines, US Patent 6,590,424 granted July 8, 2003.

RESEARCH PUBLICATIONS

DISSERTATIONS

- M. Singh. *The Design of High-Throughput Asynchronous Pipelines.* Ph.D. Thesis, Columbia University, New York, NY, December 2001.
- M. Singh. *Genetic Algorithms for the Subgraph Isomorphism Problem.* B.Tech. Thesis, Indian Institute of Technology, New Delhi, India, May 1993.

JOURNAL ARTICLES (in preparation; imminent submission)

- "An Adaptively-Pipelined Mixed Synchronous-Asynchronous Digital FIR Filter." To be submitted Spring 2007 to *Journal of Solid-State Circuits (JSSC).*
- "Low-Overhead Testing of Ultra-High-Speed Asynchronous Pipelines." To be submitted Spring 2007 to *IEEE Trans. on Computer-Aided-Design of Integrated Circuits and Systems (TCAD).*
- "High-Speed Non-Linear Asynchronous Pipelines." To be submitted Spring 2007 to *IEEE Trans. on VLSI Systems (TVLSI).*

JOURNAL ARTICLES (published, refereed)

- M. Singh and S.M. Nowick. "The Design of High-Performance Dynamic Asynchronous Pipelines: Lookahead Style." To appear in *IEEE Transactions on VLSI Systems (TVLSI)*, 14 pages, accepted November 2006.

- M. Singh and S.M. Nowick. "The Design of High-Performance Dynamic Asynchronous Pipelines: High-Capacity Style." To appear in *IEEE Transactions on VLSI Systems (TVLSI)*, 14 pages, accepted November 2006.

- M. Singh and S.M. Nowick. "MOUSETRAP: High-Speed Transition-Signaling Asynchronous Pipelines." To appear in *IEEE Transactions on VLSI Systems (TVLSI)*, 14 pages, accepted October 2006.

- M. Singh and S.M. Nowick. "Synthesis for Logical Initializability of Synchronous Finite State Machines." *IEEE Transactions on VLSI Systems (TVLSI)*, vol. 8, no. 5, pages 542-557, October 2000.

- M. Singh, A. Chatterjee, and S. Chaudhury. "Matching Structural Shape Descriptions Using Genetic Algorithms." *Pattern Recognition*, vol. 30, no. 9, pages 1451-1462, September 1997 (Elsevier Science, UK).

CONFERENCE PAPERS (published, refereed)

- G. Gill, J. Hansen and M. Singh. "Loop Pipelining for High-Throughput Stream Computation Using Self-Timed Rings." *Proc. of Intl. Conf. on Computer-Aided Design (ICCAD-06)*, San Jose, CA, November 2006.

- M. Ampalam and M. Singh. "Counterflow Pipelining: Architectural Support for Preemption in Asynchronous Systems using Anti-Tokens." *Proc. of Intl. Conf. on Computer-Aided Design (ICCAD-06)*, San Jose, CA, November 2006.

- G. Gill, A. Agiwal, M. Singh, F. Shi, and Y. Makris. "Low-Overhead Testing of Delay Faults in High-Speed Asynchronous Pipelines." *Proc. of the 12th IEEE Intl. Symp. on Async. Circ. and Syst. (ASYNC-06)*, Grenoble, France, March 2006.

- A. Agiwal and M. Singh. "An Architecture and Wrapper Synthesis for Multi-Clock Latency-Insensitive Systems." *Proc. of Intl. Conf. on Computer-Aided Design (ICCAD-05)*, San Jose, CA, November 2005.

- F. Shi, Y. Makris, S.M. Nowick and M. Singh. "Test Generation for Ultra-High-Speed Asynchronous Pipelines." *Proc. of Intl. Test Conference (ITC-05)*, Austin, TX, November 2005.

- J. Hensley, T. Scheuermann, G. Coombe, A. Lastra and M. Singh. "Fast Summed-Area Table Generation and its Applications." *Proc. of Eurographics 2005*, Dublin, Ireland, August 2005.

- J. Hensley, M. Singh, A. Lastra. "A Fast, Energy-Efficient Z-Comparator." *Proc. of the ACM SIGGRAPH/EUROGRAPHICS Conference on Graphics Hardware (GHW-05)*, Los Angeles, CA, July 2005.

- A. Agiwal and M. Singh. "Multi-Clock Latency-Insensitive Architecture and Wrapper Synthesis." *Proc. of the Second Intl. Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Design (FMGALS-05)*, in cooperation with ACM SIGDA and SIGARCH, Verona, Italy, July 2005. Published in Electronic Notes in Theoretical Computer Science, vol. 146, no. 2, January 2006. (ISSN: 1571-0661, Elsevier)

- J. Hensley, A. Lastra and M. Singh. "A Scalable Counterflow-Pipelined Asynchronous Radix-Four Booth Multiplier." *Proc. of the 11th IEEE Intl. Symp. on Async. Circ. and Syst. (ASYNC-05)*, New York City, NY, March 2005.

- J. Hensley, A. Lastra and M. Singh. "An Area- and Energy-Efficient Asynchronous Booth Multiplier for Mobile Devices." *Proc. of IEEE Intl. Conf. on Computer Design (ICCD-04)*, San Jose, CA, October 2004.

- M. Singh and M. Theobald. "Generalized Latency-Insensitive Systems for Single-Clock and Multi-Clock Architectures." *Proc. of ACM/IEEE Design, Automation and Test in Europe (DATE-04)*, Paris, France, February 2004.

- M. Singh, J.A. Tierno, A. Rylyakov, S. Rylov, and S.M. Nowick. "An Adaptively-Pipelined Mixed Synchronous-Asynchronous Digital FIR Filter Chip Operating at 1.3 Gigahertz." *Proc. of the 8th IEEE Intl. Symp. on Async. Circ. and Syst. (ASYNC-02)*, Manchester, UK, April 2002. **(Best Paper Finalist)**

- R.O. Ozdag, M. Singh, P.A. Beerel, and S.M. Nowick. "High-Speed Non-Linear Asynchronous Pipelines." *Proc. of Design, Automation and Test in Europe (DATE-02)*, Paris, France, March 2002.

- J. Tierno, A. Rylyakov, S. Rylov, M. Singh, P. Ampadu, S.M. Nowick, M. Immediato, and S. Gowda. "A 1.3 GSample/s 10-tap Full-rate Variable-latency Self-timed FIR filter with Clocked Interfaces." *Proc. of IEEE Intl. Solid-State Circ. Conf. (ISSCC-02)*, San Francisco, CA, February 2002.

- M. Singh and S.M. Nowick. "MOUSETRAP: Ultra-High-Speed Transition-Signaling Asynchronous Pipelines." *Proc. of IEEE Intl. Conf. on Computer Design (ICCD-01)*, Austin, TX, September 2001.

- M. Singh and S.M. Nowick. "High-Throughput Asynchronous Pipelines for Fine-Grain Dynamic Datapaths." *Proc. of the 6th IEEE Intl. Symp. on Adv. Res. in Async. Circ. and Syst. (ASYNC-2000)*, Eilat, Israel, April 2000. **(Received Best Paper Award)**

- M. Singh and S.M. Nowick. "Fine-Grain Pipelined Asynchronous Adders for High-Speed DSP Applications." *Proc. of IEEE Computer Society Annual Workshop on VLSI (WVLSI-2000)*, pp. 111-118, Orlando, FL, April 2000. (IEEE Computer Society Press, ISBN: 0-7695-0534-1)

- M. Singh and S.M. Nowick. "Synthesis for Logical Initializability of Synchronous Finite State Machines." *Proc. of the Tenth Intl. Conf. on VLSI Design (VLSID-97)*, Hyderabad, India, January 1997.

- M. Singh and S.M. Nowick. "Synthesis for Initializability of Asynchronous Sequential Machines." *Proc. of the Intl. Test Conference (ITC-96)*, Washington, DC, October 1996.

WORKSHOP PAPERS (refereed, limited distribution in workshop proceedings)

- G. Gill and M. Singh. "Robust Synthesis of Asynchronous Burst-Mode Machines." *Proc. of the 14th Intl. Workshop on Logic and Synthesis (IWLS-05),* Lake Arrowhead, CA, June 2005.

- G. Gill and M. Singh. "Synthesizing Asynchronous Burst-Mode Machines without the Fundamental-Mode Timing Assumption." *Proc. of the ACM/IEEE Intl. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU-05),* San Francisco, CA, February 2005.

- M. Singh and M. Theobald. "Generalized Latency-Insensitive Systems for GALS Architectures." *Proc. of the Workshop on Formal Methods for Globally Asynchronous Locally Synchronous (GALS) Architecture (FMGALS-03),* held in conjunction with the 12th International Formal Methods Europe Symposium, Pisa, Italy, September 2003.

- M. Singh and S.M. Nowick. "MOUSETRAP: Ultra-High-Speed Transition-Signaling Asynchronous Pipelines." *Proc. of the ACM/IEEE Intl. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU-2000),* Austin, TX, December 2000.

- Stephen B. Furber, A. Efthymiou and M. Singh. "A Power-Efficient Duplex Communication System." *Workshop on Asynchronous Interfaces: Tools, Techniques and Implementations*, TU Delft, the Netherlands, July 2000.

- Montek Singh and Steven M. Nowick. "State Assignment for Initializability of Synchronous Finite State Machines." *IEEE Intl. Test Synthesis Workshop (ITSW-06),* Santa Barbara, CA, May 1996.

POSTERS, SKETCHES and ABSTRACTS (refereed)

- J. Hensley, T. Scheuermann, M. Singh, and A. Lastra. "Fast Summed-Area Table Generation for Glossy Environmental Reflections," Sketch presented at SIGGRAPH 2005, Los Angeles, CA, August 2005.

- J. Hensley, T. Scheuermann, M. Singh, and A. Lastra. "Fast, Approximate HDR Image-Based Lighting Using Summed-Area Tables." Poster to be presented at Symposium on Interactive 3D Graphics and Games (i3D-07), Seattle, WA, April 2007.

- G. Gill and M. Singh. "Ray Tracing on Asynchrounous Supercomputing Stream Processors." Poster presented at the IEEE Symposium on Interactive Ray Tracing, Salt Lake City, Utah, September 2006.

- G. Gill, J. Hansen and M. Singh. "High-Throughput Looping in Stream Processors Using Self-Timed Architectures." Poster and abstract at the Workshop on Edge Computing Using New Commodity Architectures (EDGE), Chapel Hill, NC, May 2006.

- M. Singh, "The Design of High-Speed Asynchronous Pipelines." Poster presented at the ACM SIGDA Ph.D. Forum, held in conjunction with the Design Automation Conference (DAC-01), Las Vegas, NV, June 2001.

WORKSHOP PAPER (not refereed, limited distribution in workshop proceedings)

- Montek Singh and Steven M. Nowick, "Gate-Level Pipelines for High Throughput." *Proc. of the 6th UK Asynchronous Forum*, Manchester, UK, July 1999.

PROFESSIONAL ACTIVITIES

CONFERENCE ACTIVITIES

- Program Committee Co-Chair, *13th International Symposium on Asynchronous Circuits and Systems (ASYNC-07)*, Berkeley, CA, March 2007.
- Program Committee Co-Chair, *2nd International Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Design (FMGALS-05)*, Verona, Italy, July 2005.
- Publicity Co-Chair, *12th International Symposium on Asynchronous Circuits and Systems (ASYNC-06)*, Grenoble, France, March 2006.
- Local Arrangements Co-Chair, *11th International Symposium on Asynchronous Circuits and Systems (ASYNC-05)*, New York, NY, March 2005.
- Publicity Chair, *11th International Symposium on Asynchronous Circuits and Systems (ASYNC-05)*, New York, NY, March 2005.
- Invited Speakers Chair, ASYNC 2003 *9th International Symposium on Asynchronous Circuits and Systems (ASYNC-03)*, Vancouver, Canada, May 2003.

TECHNICAL PROGRAM COMMITTEES

- 13th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2007
- ACM/IEEE Design, Automation and Test in Europe (DATE), 2007
- ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2007
- IEEE International Conference on Computer Design (ICCD), 2006
- 12th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2006
- ACM/IEEE Design, Automation and Test in Europe (DATE), 2006
- ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2006
- IEEE International Conference on Computer Design (ICCD), 2005
- 2nd Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Architectures (FMGALS), 2005

- 11th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2005
- ACM/IEEE Design, Automation and Test in Europe (DATE), 2005
- ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2005
- 10th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2004
- ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2004
- 1st Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Architectures (FMGALS), 2003
- 9th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2003
- 8th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2002
- ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2002

OTHER CONFERENCE ACTIVITIES

- Session Chair, "Optimization," ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2002
- Session Chair, Keynote Session, 9th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2003
- Session Chair, "Design and Test," 10th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2004

GOVERNMENT REVIEW PANELS

(Dates and program names not provided to ensure confidentiality.)

- NSF proposal review panel, 2004
- NSF proposal review panel, 2005

JOURNAL AND CONFERENCE REFEREEING

- IEEE Transactions on Circuits and Systems (TCAS)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on VLSI (TVLSI)
- IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)
- Design Automation Conference (DAC)
- European Solid-State Circuits Conference (ESSCIRC)
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI)
- IEEE/ACM International Workshop on Logic and Synthesis (IWLS)
- Conference on Advanced Research in VLSI (ARVLSI)
- International Conference on Computer Design (ICCD)
- IEE Proceedings
- Microprocessors and Microelectronics Journal (M&M)

PROFESSIONAL SOCIETY MEMBERSHIPS

- IEEE Computer Society
- ACM SIGDA (Design Automation)

INVITED TALKS

- **Duke University,** Durham, NC: "Design of Asynchronous Pipelined Systems," February 2007. Host: Prof. Krish Chakrabarty.
- **Achronix Semiconductor/Cornell University:** "Design of Asynchronous Pipelined Systems," January 2007. Host: Prof. Rajit Manohar.
- **Univ. of British Columbia**, Vancouver, Canada: "Design of Asynchronous Pipelined Systems," January 2007. Host: Prof. Mark Greenstreet.
- **IBM T. J. Watson Research Center,** Yorktown Heights, NY: "Design of Asynchronous Pipelined Systems," December 2006. Host: Dr. Jose Tierno.
- **Columbia University,** New York, NY: "Design of Asynchronous Pipelined Systems," December 2006. Host: Prof. Steven Nowick.
- **Univ. of Utah,** Salt Lake City, Utah: "Design of Asynchronous Pipelined Systems," November 2006. Hosts: Prof. Al Davis and Prof. Erik Brunvand.
- **Univ. of Southern California,** Los Angeles, CA: "Design of Asynchronous Pipelined Systems," November 2006. Host: Prof. Peter Beerel.
- **Univ. of California, Berkeley,** CA: "Design of Asynchronous Pipelined Systems," November 2006. Hosts: Dr. Marly Roncken and Dr. Ivan Sutherland.
- **Sun Microsystems Laboratories,** Mountain View, CA: "Design of Asynchronous Pipelined Systems," November 2006. Host: Dr. Jo Ebergen.
- **IBM T. J. Watson Research Center,** Yorktown Heights, NY: "Grappling with Latency in the Nanoscale Era," October 29, 2004. Host: Dr. Jose Tierno.
- **Columbia University,** New York, NY: "Challenges in Hardware Design in the Nanoscale Era," Mar 22, 2004. Host: Prof. Steven M. Nowick.
- **DARPA Clockless Logic Workshop,** San Jose, CA: "High-Level Synthesis of Asynchronous and Mixed-Timing Digital Systems," September 2003. Host: Dr. Robert Reuss.
- **University of California, Davis,** CA: "The Design of High-Speed Asynchronous Pipelines," May 4, 2001. Host: Prof. Jonathan Heritage.
- **Georgia Institute of Technology,** Atlanta, GA: "The Design of High-Speed Asynchronous Pipelines," April 2, 2001. Host: Prof. David E. Schimmel.
- **Univ. of North Carolina at Chapel Hill,** Chapel Hill, NC: "The Design of High-Speed Asynchronous Pipelines," March 26, 2001. Host: Prof. Gary Bishop.
- **Brown University,** Providence, RI: "The Design of High-Speed Asynchronous Pipelines," March 19, 2001. Host: Prof. Harvey Silverman.
- **Sun Microsystems Laboratories,** Mountain View, CA: "The Design of High-Throughput Asynchronous Pipelines," November 9, 2000. Host: Dr. Jo Ebergen.

- **Stanford University,** Palo Alto, CA: "The Design of High-Throughput Asynchronous Pipelines," November 8, 2000. Host: Prof. Mark Horowitz.
- **Stanford University,** Palo Alto, CA: "The Design of High-Throughput Asynchronous Pipelines," November 8, 2000. Host: Prof. Edward McCluskey.
- **IBM T. J. Watson Research Center,** Yorktown Heights, NY: "High-Throughput Asynchronous Pipelines for Fine-Grain Dynamic Datapaths," May 24, 2000. Host: Dr. Jose Tierno.
- **Theseus Logic,** Orlando, FL: "High-Throughput Asynchronous Pipelines for Fine-Grain Dynamic Datapaths," April 26, 2000. Hosts: David Lamb and Karl Fant.

TECHNOLOGY TRANSFER

- **IBM T.J. Watson Research Center:** *Design of a to-spec digital FIR filter chip for disk drives* (2000-2002).

  I was invited by IBM Research in August 2000 to apply one of my pipeline styles (the "high-capacity" style) to a real-world application: a to-spec design of an FIR filter chip for use in disk drives. The design was fabricated in silicon (0.18 micron), and the resulting chip exceeded performance goals, offering a 50% reduction in latency and 25% improvement in throughput (1.3 Giga samples/sec) over IBM's best synchronous implementation. This design provided an industrial-strength validation of my research.

- **Boeing and Handshake Solutions (a Philips spin-off):** *Development of a high-speed pipeline synthesis flow* (2005-present).

  I was invited in 2005 to join the DARPA CLASS program, a major ($14M) initiative in asynchronous design, to transfer another of my pipeline styles (the "MOUSETRAP" style) for potential commercial use. In particular, I am leading the effort to combine the high performance of my pipeline circuits with the industrial-strength asynchronous CAD flow called Haste, developed by Handshake Solutions (a Philips spin-off). We have successfully created an experimental automated pipeline synthesis flow for high-performance system implementation. My pipeline circuits were chosen for this project because of their uniqueness in offering high performance yet ease-of-construction. Upon successful completion and commercialization, this project has the potential to impact a large number of microelectronic companies by making asynchronous design technology available for large-scale industrial use.

TEACHING AND SERVICE

TEACHING

- *Digital Logic* (Comp541), Spring 2007: 7 students.
- *Computer Architecture* (Comp206), Fall 2005: 30 students.
- *Computer Architecture* (Comp206), Fall 2004: 25 students.
- *Computer Architecture* (Comp206), Fall 2003: 30 students.
- *Computer Architecture* (Comp206), Fall 2002: 17 students.
- *Introduction to VLSI Design* (Comp268), Spring 2005: 4 students.
- *Clockless Computing and Silicon Compilers* (Comp290), Spring 2006: 7 students.
- *Asynchronous Systems and Introduction to VLSI Design* (Comp290), Spring 2004: 7 students.
- *Introduction to Asynchronous Design* (Comp290), Spring 2003: 4 students.
- *High-Speed Asynchronous Pipelines* (Comp290), Fall 2001: 7 students and 3 faculty.
- *Elements of Hardware Systems* (Comp261), co-taught with Lea Vicci, Spring 2002: 7 students.

DEPARTMENT COMMITTEES

- Graduate Admissions Committee (2002-2007)
- Ad-Hoc Qualifying Exam Restructuring Committee (Spring 2003)
- Ad-Hoc Undergraduate Hardware Curriculum Committee (Fall 2002)

PH.D. STUDENTS GRADUATED

- **Justin Hensley** (Fall 2003-Fall 2006), joint with Prof. Anselmo Lastra: Graduated with Ph.D. degree; employed by AMD/ATI. Ph.D. Thesis: *Improving the Rendering Quality of Graphics Hardware.*

M.S. STUDENTS GRADUATED

- **Manoj Ampalam** (Fall 2005-Spring 2006): Graduated with M.S. degree; employed by Microsoft Research. M.S. Thesis: *Counterflow Pipelining for Preemption in Asynchronous Systems.*
- **Ankur Agiwal** (Fall 2004-Fall 2005): Graduated with M.S. degree; employed by Microsoft Research.

CURRENT PH.D. STUDENTS

- **Gennette Gill** (Fall 2003-present). Research topic: Design, optimization and testing of large-scale asynchronous systems.
- **John Hansen** (Fall 2005-present). Research topic: Silicon compilers for high-performance asynchronous design.
- **Vishal Gupta** (Fall 2006-present). Research topic: Optimization and formal verification of counterflow pipelines with anti-tokens.

OTHER STUDENTS SUPERVISED

- Todd Gamblin (Fall 2003-Spring 2004).
- Sushant Rewaskar (Fall 2002-Spring 2003).

PH.D. PROPOSAL COMMITTEES (external)

- Lara Oliver, Ph.D. proposal committee, Duke University, December 2006.
- Sudarshan Bahukudumbi, Ph.D. proposal committee, Duke University, March 2007.

OTHER MENTORING ACTIVITIES

- ACM programming team coach (joint with Prof. Kevin Jeffay): Fall 2003.
- Faculty advisor to Bhangra Elite, a campus South-Asian nationally-competitive dance team: Fall 2004-present.
- Faculty advisor to Tamasha, a campus South-Asian cultural and outreach organization: Fall 2005-present.