COMP 160 Lab 2, Designing a Decoder

The goals of this lab are to do a little more Verilog design and to write a simple Verilog testbench.

You will design a Hex-to-Seven-Segment decoder. There is a good explanation of a similar decoder in your book, Logic and Computer Design Fundamentals 3rd edition, on page 107. The only difference between the decoder in your book and the one you are going to design is that you are not stopping at 9 as an output value, but rather at hexadecimal F. You will be able to use this decoder to debug circuits you design later. For more on simple Verilog and a decoder design, refer to page 184 in the book.

Connect the inputs of the decoder to the DIP switches.

Test by writing a Verilog test program (to try all possible inputs) and simulating. Then assign pins and download to the Xess board to make a final test/

Useful pinout information (from the XSA manual)

Seven-Segment Display

Top, s[6]	P49
Upper Left, s[5]	P57
Upper Right, s[4]	P46
Middle, s[3]	P60
Lower Left, s[2]	P62
Lower Right, s[1]	P39
Bottom, s[0]	P67

DIP switches (normally high)

1	P54
2	P64
3	P63
4	P56

Mail the instructor and TA copies of your decoder Verilog and of your test program.