COMP160 - Lab 3

Sequential Design: A Digital Lock

This is the first sequential design assignment. The task is to design and implement an electronic lock for a door.

I'd also like you to use the logic analyzer. First use it to see what frequency the clock on your Xess board is generating. You can also check to see if the lower frequency you expect from the clock divider is what you actually got (see below)

The input combination is a sequence of three 4-bit digits. You have four switches and a pushbutton. Set the switches to the first number of the combination, press the button, change the switches to the second number, press the button, etc. If you successfully enter the appropriate three numbers, a signal goes high to unlock the door (in your case, to light one of the LEDs). The correct combination can be encoded as part of the design.

You will also want some way to reset the lock. Perhaps it resets when you press the button again after the door has closed. A second button can also generate this signal. If the reset signal goes high, the door locks. I'll leave some buttons and resistors for you to use. An alternative to a reset switch is to *time out* after a given period of time has passed.

Your assignment is as follows.

1. This specification was vague; such as you might get from a client. Formalize the specification with truth tables or logic equations. Justify any design decisions that you make.

2. Code the design in Verilog and simulate it. Give a justification for your choice of test sequence. Why does it do a good job of testing the design?

3. Download the design onto the Xess board. Demonstrate your working design, if possible.

Email the following

1. A design document, with the design decisions you have made and justification for those.
2. The project itself as a zip file.
3. Simulation results.

More Details

For this assignment you'll need a clock running at a modest frequency. You'll need to divide the clock provided on the XSA-100 board down to some frequency more useful for this task. We provided some Verilog to generate a slower clock.

You can use the pushbutton on the board but you'll need some logic to synchronize it with the clock and debounce it. We've talked about this in class.

The XSA-100 board clock is on pin 88 of the FPGA.

Other useful pin information (from the schematic diagram):

Seven-Segment Display	
Top, s[6]	P49
Upper Left, s[5]	P57
Upper Right, s[4]	P46
Middle, s[3]	P60
Lower Left, s[2]	P62
Lower Right, s[1]	P39
Bottom, s[0]	P67
Pushbutton (normally high)	P93
DIP switches (normally high)	
1	P54
2	P64
3	P63
4	P56

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