COMP 160 Lab 4 – VGA Timing Generator

Design a module that generates VGA timing signals. For now you can test by making a higher-level module to display something interesting, like contrasting vertical lines, colored blocks, etc. Later you'll use this to build a character display.

Please see the lecture notes for details.

I suggest that you proceed as follows.

1. First build a horizontal counter with a shorter count than you'd use for VGA, and test it on the simulator. Note that the only input is a clock, which you may want to count down to 25 MHz.
2. Add an hsync signal and simulate it (you may want to simulate it with less than 640 pixels).
3. Use the horizontal counter to build a vertical (scan line) counter and test that design.
4. Finally, set your parameters for an actual VGA scan and try it on a CRT.

If you have any problems, use the logic analyzer to see what you are sending to the display. Even if you have no trouble with the design, I encourage you to try the logic analyzer.

Report

Demo the VGA generator.

Send a report by the deadline. It should include your project as a Zip file, and a short description of how you arrived at the design and your simulation/test strategy. Please include a copy of the Verilog code in the document so I can read it easily without running your ISE project.

In the report, list the resources used by your design. First list the high-level resources: counters and FSMs. Then the number of FPGA slices.