IMAGE-COMPOSITION ARCHITECTURES FOR REAL-TIME IMAGE GENERATION

by

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STEVEN EDWARD MOLNAR. Image-Composition Architectures for Real-Time Image Generation (under the direction of Henry Fuchs).

ABSTRACT

This dissertation describes a new approach for high-speed image-generation based on image compositing. Application software distributes the primitives of a graphics database over a homogeneous array of processors called renderers. Each renderer transforms and rasterizes its primitives to form a full-sized image of its portion of the database. A hardware datapath, called an image-composition network, composites the partial images into a single image of the entire scene.

Image-composition architectures are linearly scalable to arbitrary performance. This property arises because: 1) renderers compute their subimages independently, and 2) an image-composition network can accommodate an arbitrary number of renderers, with constant bandwidth in each link of the network. Because they are scalable, image-composition architectures promise to achieve much higher performance than existing commercial or experimental systems. They are flexible as well, supporting a variety of primitive types and rendering algorithms. Also, they are efficient, having approximately the same performance/price ratio as the underlying renderers.

Antialiasing is a special challenge for image-composition architectures. The compositing method must retain primitive geometry within each pixel to avoid aliasing. Two alternatives are explored in this dissertation: simple *z*-buffer compositing combined with supersampling, and A-buffer compositing.

This dissertation describes the properties of image-composition architectures and presents the design of a prototype *z*-buffer–based system called PixelFlow. The PixelFlow design, using only proven technology, is expected to render 2.5 million triangles per second and 870 thousand antialiased triangles per second in a two-card–cage system. Additional card cages can be added to achieve nearly linear increases in performance.

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LIST OF ABBREVIATIONS

ALU	Arithmetic Logic Unit
BSP	Binary Space Partitioning
CRT	Cathode Ray Tube
DMA	Direct Memory Access
DRAM	Dynamic Random-Access Memory
EMC	Enhanced Memory Chip
FIFO	First-In-First-Out (queue)
GHz	gigahertz (10^9 Hz)
GP	Graphics Processor
Gbit	gigabit (10^9 or 2^{30} bits)
Gbyte	gigabyte (10^9 or 2^{30} bytes)
Gword	gigaword (10^9 words)
Hz	hertz (cycles per second)
I/O	input/ouput
IGC	Image Generation Controller
Kbit	kilobit (10^3 or 2^{10} bits)
Kbyte	kilobyte (10^3 or 2^{10} bytes)
LSB	least-significant bit (or byte)
MFLOPS	million floating-point operations per second
MHz	megahertz (10^6 Hz)
MIP	*multum in parvo* (multi-resolution table for filtering textures)
MIPS	million instructions per second
MSB	most-significant bit (or byte)
Mbit	megabit (10^6 or 2^{20} bits)
Mbyte	megabyte (10^6 or 2^{20} bytes)
Mword	megaword (10^6 words)
NURB	Non-Uniform Rational B-Spline
PC	printed-circuit (board)
PLD	Programmable Logic Device
RGB	Red/Green/Blue
RGBα	Red/Green/Blue/Alpha
RISC	Reduced Instruction Set Computer
SIMD	Singe-Instruction Multiple-Data
TLB	Translation Lookaside Buffer
U	Height-unit (1.75 inches—for PC boards)
VRAM	Video Random-Acess Memory
mil	10^{-3} inches
msec	millisecond (10^{-3} seconds)
***n*-T**	*n*-transistor (in a memory cell)
nsec	nanosecond (10^{-9} seconds)
tri	triangle
μ**sec**	microsecond (10^{-6} seconds)