November 28

- 3 classes to go
- Next 2 classes devoted to review and your questions
- No questions →no class
- Know answers or no pass!

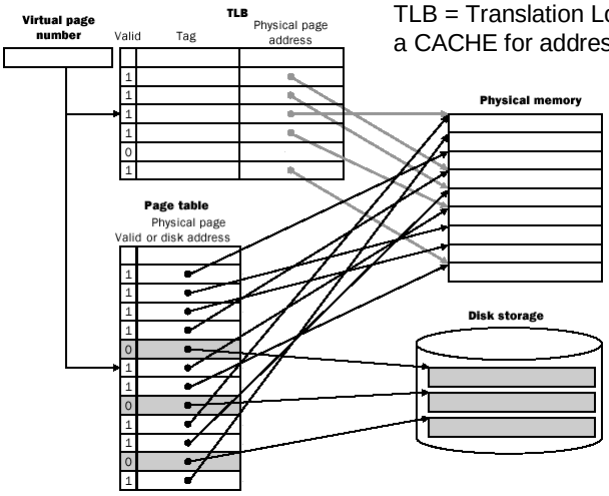
Address Translation

- Instruction Fetch
  - Use PC to get VIRTUAL address
  - Lookup VIRTUAL address in TLB
    - MISS → OS Trap
  - Lookup PHYSICAL address in INSTRUCTION CACHE
    - MISS → STALL waiting on MEMORY
  - Finally deliver instruction to INSTRUCTION REGISTER

Address Translation

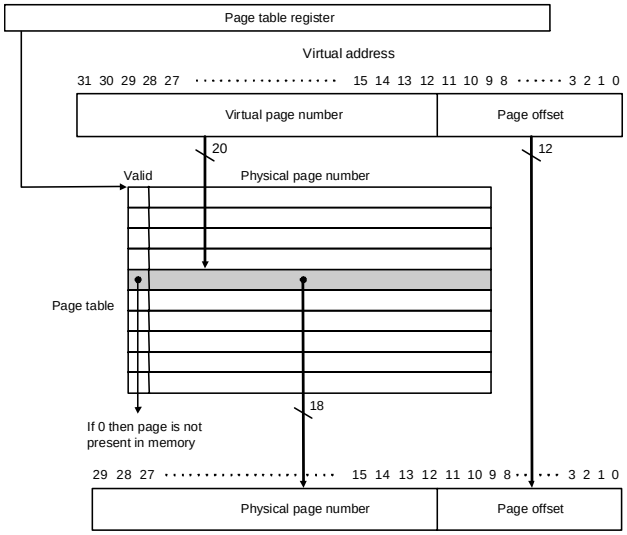
- Data Fetch
  - Use PC to get VIRTUAL address
  - Lookup VIRTUAL address in TLB
    - MISS → OS Trap
  - Lookup PHYSICAL address in L1 DATA CACHE
    - MISS → STALL waiting on L2 DATA CACHE
  - Lookup PHYSICAL address in L2 DATA CACHE
    - MISS→ STALL waiting on memory
  - Finally Deliver data to the STALLED pipeline

Making Address Translation Fast



TLB = Translation Lookaside Buffer
a CACHE for address translation

Virtual Address Translation



16k direct-mapped cache

- 16 byte BLOCKS
- How many BLOCKS?
- Which bits to select the BLOCK?
- How many bits in the TAG?

Direct-Mapping Example

•With 8 byte BLOCKS, the bottom 3 bits determine the byte in the BLOCK

•With 4 cache BLOCKS, the next 2 bits determine which BLOCK to use

1024d = 10000000000b → line = 00b = 0d

1000d = 01111101000b → line = 01b = 1d

1040d = 10000010000b → line = 10b = 2d

Tag	Data	
1024	44	99
1000	17	23
1040	1	4
1016	29	38

Memory

1000	17
1004	23
1008	11
1012	5
1016	29
1020	38
1024	44
1028	99
1032	97
1036	25
1040	1
1044	4

Direct Mapping Miss

•What happens when we now ask for address 1008?

1008d = 01111110000b → line = 10b = 2d

but earlier we put 1040d there...

1040d = 10000010000b → line = 10b = 2d

Tag	Data	
1024	44	99
1000	17	23
1008	11	5
1016	29	38

Memory

1000	17
1004	23
1008	11
1012	5
1016	29
1020	38
1024	44
1028	99
1032	97
1036	25
1040	1
1044	4

8k 2-way Set Associative Cache

- With 32 byte BLOCKS
- How many BLOCKS?
- Which bits select the (pair of) BLOCKs?
- How many bits in the TAG?

Classes to go

2