

October 10

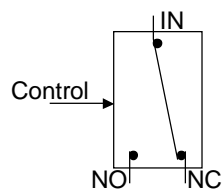
- Chapter 4 – Logic Gates
- Read in Chapter 4 pages 250-258, 265-274, section 4.8 through top of page 288, section 4.10

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Ideal Switch



When Control == 0

NC == IN (NC is connected to IN)

When Control == 1

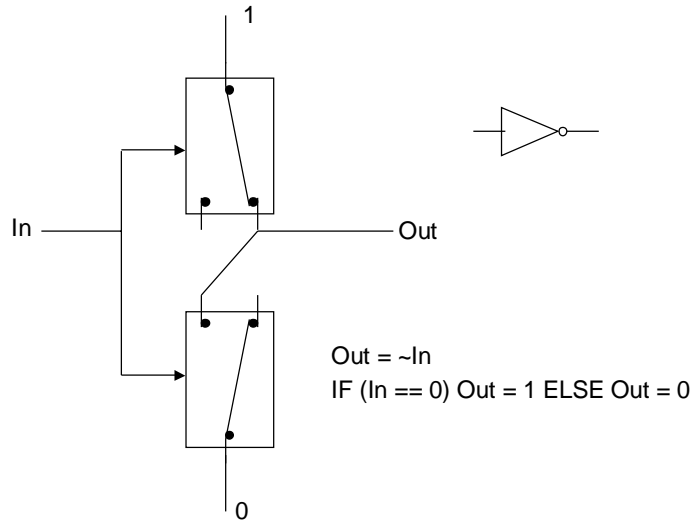
NO == IN (NO is connected to IN)

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Inverter

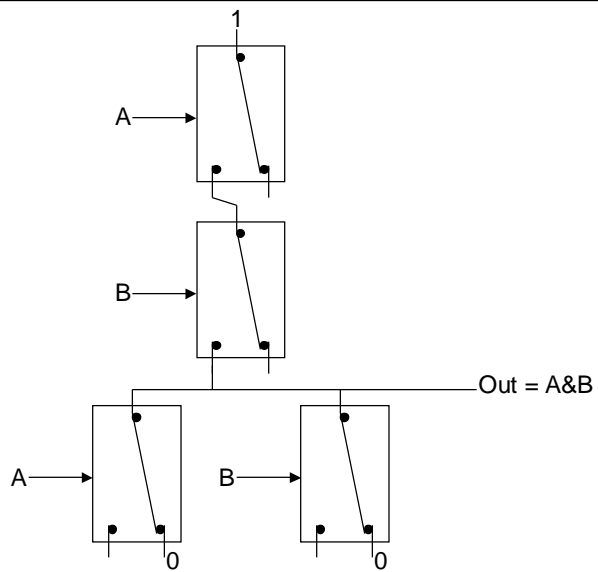


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AND

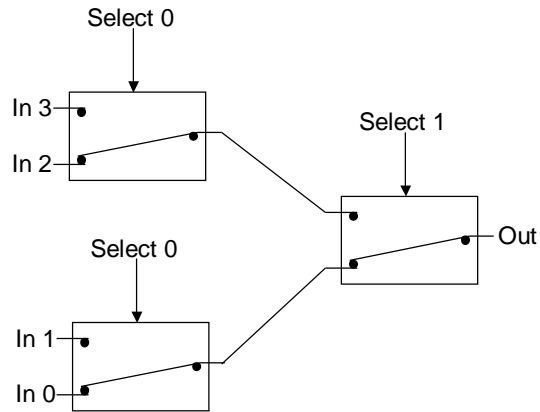


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4-input MUX



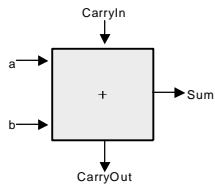
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1-bit ALU for Addition

- Let's look at implementing our 1-bit adder with gates



$$\begin{aligned}
 c_{out} &= a \& b \mid a \& c_{in} \mid b \& c_{in} \\
 sum &= a \& \sim b \& \sim c_{in} \mid \sim a \& b \& \sim c_{in} \\
 &\quad \mid \sim a \& \sim b \& c_{in} \mid a \& b \& c_{in}
 \end{aligned}$$

a	b	cin	sum	cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

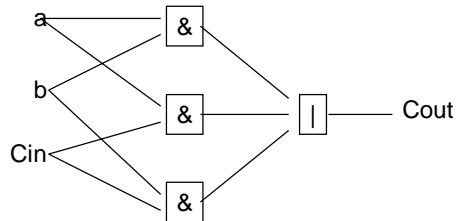
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Cout in Gates

$$c_{out} = a \& b \mid a \& c_{in} \mid b \& c_{in}$$



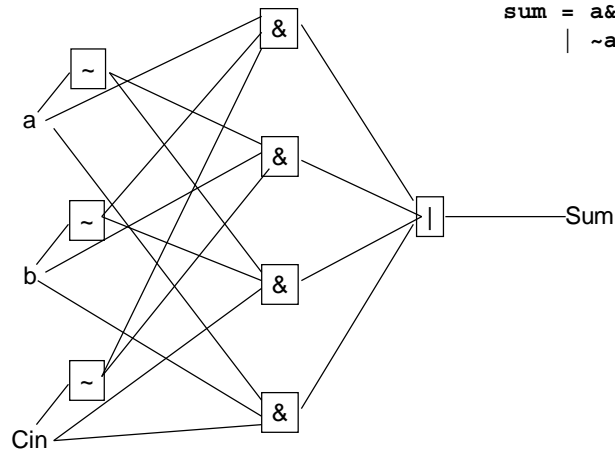
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Sum in Gates

$$\text{sum} = a \& \sim b \& \sim c_{in} \mid \sim a \& b \& \sim c_{in} \mid \sim a \& \sim b \& c_{in} \mid a \& b \& c_{in}$$



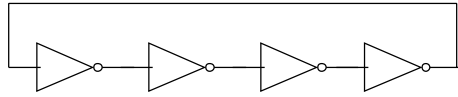
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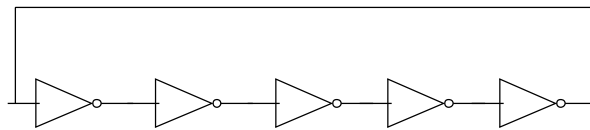
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How Fast?

What does this do?



How about this?

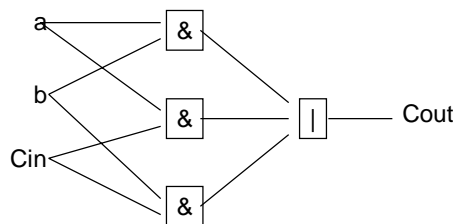


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How many gate delays for Cout?



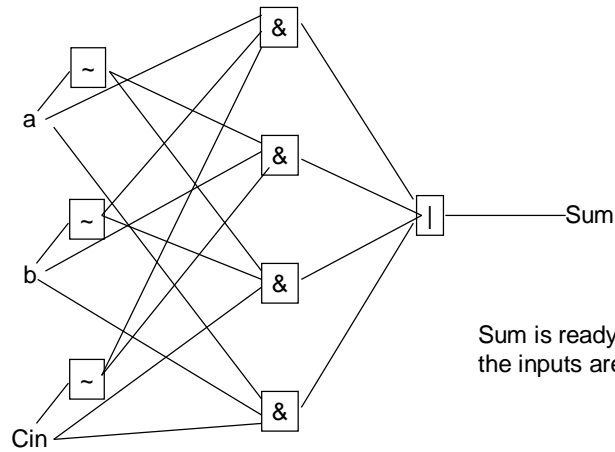
Cout is ready 2 gate delays after the inputs are ready

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How many gate delays for Sum?



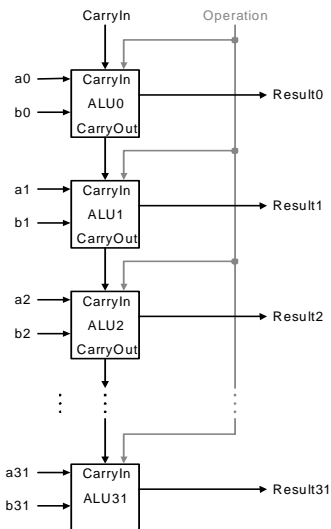
Sum is ready 3 gate delays after the inputs are ready

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How slow can you go?



Cin for ALU31 is ready 62 gate delays after the initial input was ready
 Result31 will be ready 3 gate delays later for a total of 65 gate delays

If a gate delay is 1ns what is the fastest clock rate for addition to happen in 1 cycle?

What about AND?

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