

26 October

- Only 11 to go!
- Questions?
- Today Exam Review and Instruction Execution

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[10] How many bits are required to store a 10-digit number (i.e. a phone number that might range from 0000000000 to 9999999999) as a binary integer? As ASCII characters?

$$10^{10} = 10 * 10^9 = 10 * 2^{30} < 2^{34} = 34 \text{ bits}$$

$$10 \text{ characters} * 8 \text{ bits/character} = 80 \text{ bits}$$

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[5] Suppose the byte at location 1000 in memory contains the hex value 0x87. What is the content of register \$t0 after the instruction "lb \$t0,1000(\$zero)"? What is its content after the instruction "lbu \$t0,1000(\$zero)"? We're comparing the "load byte" instruction to the "load byte unsigned" instruction.

The lb instruction will "sign extend" so the result will be 0xffff87 while the lbu will produce 0x00000087

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[10] Which of the following **cannot** be EXACTLY represented by an IEEE double-precision floating-point number?

- (a) 0
- (b) 10.2
- (c) 1.625
- (d) 11.5

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[12] All of the following equations are true for the idealized numbers you studied in algebra. Which ones are true for IEEE floating point numbers? Assume that all of the numbers are well within the range of largest and smallest possible numbers (that is, underflow and overflow are not a problem)

- $A+B=A$ if and only if $B=0$
- $(A+B)+C = A+(B+C)$
- $A+B = B+A$
- $A*(B+C) = A*B+A*C$

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[12] Consider the characteristics of two machines M1 and M2. M1 has a clock rate of 1GHz. M2 has a clock rate of 2GHz. There are 4 classes of instructions (A-D) in the instruction set. In a set of benchmark programs, the frequency of each class of instructions is shown in the table.

Instruction Class	Frequency	M1 CPI	M2 CPI
A	40%	2	6
B	25%	3	6
C	20%	3	6
D	15%	5	8

What is the average CPI for each machine? Which machine is faster? By what factor faster is it? What is the cycle time of each machine?

$$CPI1 = 2*0.4+3*0.25+3*0.2+5*0.15 = 2.9$$

$$CPI2 = 6*0.4+6*0.25+6*0.2+8*0.15 = 6.3$$

$$M1 \text{ is faster by } (1000/2.9) / (2000/6.3) = 1.086$$

$$M1 \text{ cycle time} = 1\text{ns}, M2 \text{ cycle time} = 0.5\text{ns}$$

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[10] How can the ALU we talked about in class be used to compare two values for equality?

Subtract (invert, add, with $C_{in}=1$) and OR the 32 bits of the result together with an additional gate. If the output of that gate is 9; then the values are equal.

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[5] Using 2's complement arithmetic, negate $0x1234ffff$. What is its value in hex?

$0x1234ffff$ inverted = $0xedcb0000$ plus 1 = $0xedcb0001$

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[10] Show, step by step, how to add -17 (negative 17) and 20 (positive 20) using 2's complement arithmetic and 8 bit integers.

17 is $0x11$, so ~ 17 is $0xee$, so ~ 17 is $0xef = 11101111$

20 is $0x14 = 00010100$

Add them bit-by-bit to get $00000011 = 0x03$

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[6] When multiplying unsigned numbers that are N bits long using the shift and add algorithm, how many additions are required on average if all multipliers are equally likely?

$N/2$

Are all multipliers equally likely?

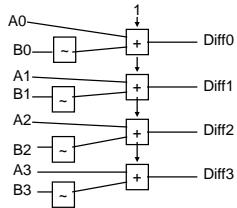
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[15] Draw a block diagram showing how to implement 2's complement subtraction of 4 bit numbers (A minus B) using 1-bit full-adder blocks with inputs A, B, and C_{in} and outputs Sum and C_{out} and any other AND, OR, or INVERT blocks you may need.

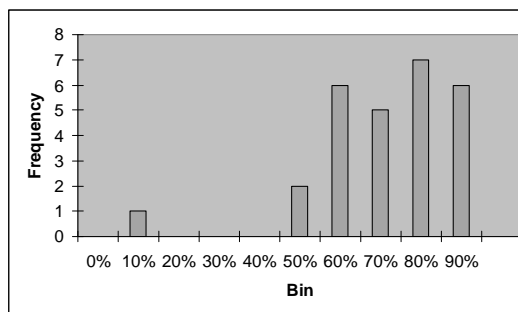


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Grade Distribution



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Instruction Execution

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Five Execution Steps

- Instruction Fetch
- Instruction Decode and Register Fetch
- Execution, Memory Address Computation, or Branch Completion
- Memory Access or R-type instruction completion
- Memory Read Completion

INSTRUCTIONS TAKE FROM 3 - 5 CYCLES!

- A FSM looks at the op-code to determine how many...

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Step 1: Instruction Fetch

- Use PC to get instruction and put it in the Instruction Register.
- Increment the PC by 4 and put the result back in the PC.
- Can be described succinctly using RTL "Register-Transfer Language"

```
IR = Memory[PC]; IR is "Instruction Register"
PC = PC + 4;
```

What is the advantage of updating the PC now?

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Step 2: Instruction Decode and Register Fetch

- Read registers rs and rt in case we need them
- Compute the branch address in case the instruction is a branch
- RTL:

```
A = Reg[IR[25-21]];
B = Reg[IR[20-16]];
ALUOut = PC + (sign-extend(IR[15-0]) << 2);
```

- We aren't setting any control lines based on the instruction type (we are busy "decoding" it in our control logic)

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Step 3 (instruction dependent)

- ALU is performing one of three functions, based on instruction type
- Memory Reference:

```
ALUOut = A + sign-extend(IR[15-0]);
```

- R-type:

```
ALUOut = A op B;
```

- Branch:

```
if (A==B) PC = ALUOut;
```

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Step 4 (R-type or memory-access)

- Loads and stores access memory

```
MDR = Memory[ALUOut]; MDR is Memory Data Register
OR
Memory[ALUOut] = B;
```

- R-type instructions finish

```
Reg[IR[15-11]] = ALUOut;
```

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Step 5 Memory Read Completion

- $\text{Reg}[\text{IR}[20-16]] = \text{MDR}$;

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Summary:

Step name	Action for R-type instructions	Action for memory-reference instructions	Action for branches	Action for jumps
Instruction fetch		$\text{IR} = \text{Memory}[\text{PC}]$		
		$\text{PC} = \text{PC} + 4$		
Instruction decode/register fetch		$A = \text{Reg}[\text{IR}[25-21]]$ $B = \text{Reg}[\text{IR}[20-16]]$		
		$\text{ALUOut} = \text{PC} + (\text{sign-extend}(\text{IR}[15-0]) \ll 2)$		
Execution, address computation, branch/jump completion	$\text{ALUOut} = A \text{ op } B$	$\text{ALUOut} = A + \text{sign-extend}(\text{IR}[15-0])$	if $(A == B)$ then $\text{PC} = \text{ALUOut}$	$\text{PC} = \text{PC} [31-28] \ll (\text{IR}[25-0] \ll 2)$
Memory access or R-type completion	$\text{Reg}[\text{IR}[15-11]] = \text{ALUOut}$	Load: $\text{MDR} = \text{Memory}[\text{ALUOut}]$ or Store: $\text{Memory}[\text{ALUOut}] = B$		
Memory read completion		Load: $\text{Reg}[\text{IR}[20-16]] = \text{MDR}$		

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