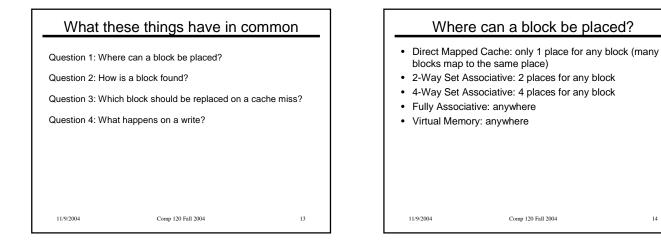
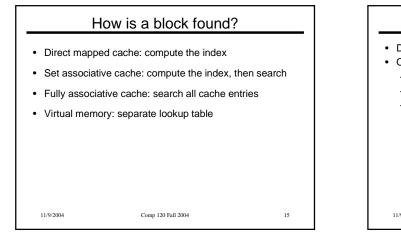
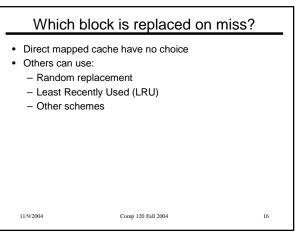


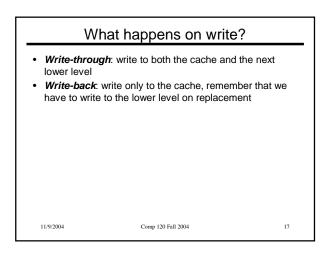
	Some Issues	
	eds continue to increase aster than either DRAM or disk access	times
Design challen	ge: dealing with this growing disparity	
 redesign DI processing restructure 	is SRAMs (provide a burst of data) RAM chips to provide higher bandwidth code to increase locality hing (make cache visible to ISA)	or
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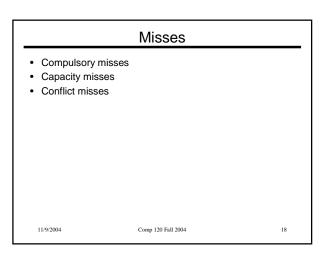






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	Classes to go	
	6	
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