16 November

• 5 classes to go
• Questions?
• More on VM and Cache

4kB Direct Mapped Cache

Address (showing bit positions):

0 1 2 3

Index 4

64kB Cache

Address (showing bit positions):

0 1 2 3

Index 4

4kB 4-way Set Associative Cache

Address (showing bit positions):

0 1 2 3

Index 4

64k direct-mapped cache

• 16 byte BLOCKS
• How many BLOCKS?
• Which bits to select the BLOCK?
• How many bits in the TAG?

4kB direct-mapped cache

• 4 byte BLOCKS
• How many BLOCKS?
• Which bits to select the BLOCK?
• How many bits in the TAG?
4kB 4-way set associative cache

Address Translation

- Instruction Fetch
  - Use PC to get VIRTUAL address
  - Lookup VIRTUAL address in TLB
    - MISS → OS Trap
  - Lookup PHYSICAL address in INSTRUCTION CACHE
    - MISS → STALL waiting on MEMORY
  - Finally deliver instruction to INSTRUCTION REGISTER

Address Translation

- Data Fetch
  - Use ALU to get VIRTUAL address
  - Lookup VIRTUAL address in TLB
    - MISS → OS Trap
  - Lookup PHYSICAL address in L1 DATA CACHE
    - MISS → STALL waiting on L2 DATA CACHE
  - Lookup PHYSICAL address in L2 DATA CACHE
    - MISS → STALL waiting on memory
  - Finally Deliver data to the STALLED pipeline

Making Address Translation Fast

Virtual Address Translation

VM meets Cache
VM meets Cache

Virtual address

- TLB access
  - Yes
  - No

- TLB miss exception

  - No
  - Update the TLB

  - Yes

- Physical address

  - No
  - Write

  - Yes

- Cache miss result

  - No
  - Cache hit

  - Yes

  - Write access

  - No

  - Write protection exception

    - No

    - Write data into cache

    - Yes

      - Update the tag, and put the data into the cache

      - No

      - Data not available

        - No

        - TLB miss exception

          - No

          - Write access

            - No

            - Physical address

              - No

              - No

              - Yes

      - Yes

    - Yes

Classes to go

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