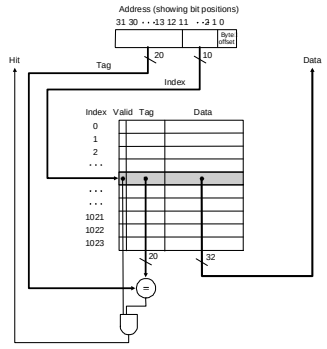
16 November

- 5 classes to go
- Questions?
- More on VM and Cache

4kB direct-mapped cache

- 4 byte BLOCKS
- How many BLOCKS?
- Which bits to select the BLOCK?
- How many bits in the TAG?

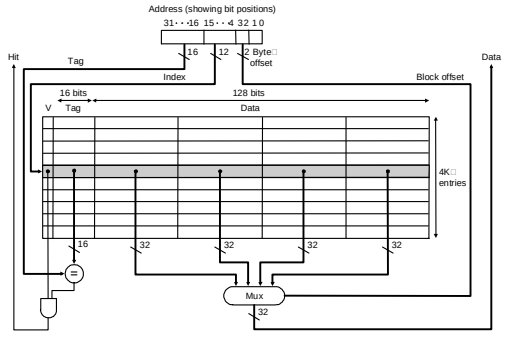
4kB Direct Mapped Cache



64k direct-mapped cache

- 16 byte BLOCKS
- How many BLOCKS?
- Which bits to select the BLOCK?
- How many bits in the TAG?

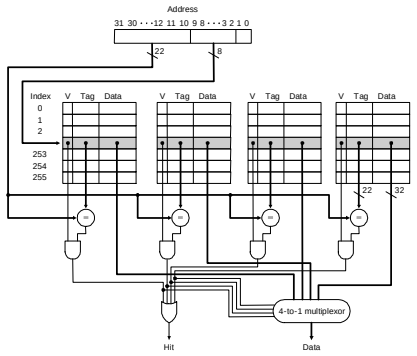
64kB Cache



4kB 4-way Set Associative Cache

- With 4 byte BLOCKS
- How many BLOCKS?
- Which bits select the BLOCKs?
- How many bits in the TAG?

4kB 4-way set associative cache



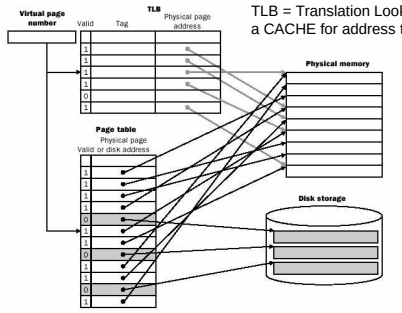
Address Translation

- Instruction Fetch
  - Use PC to get VIRTUAL address
  - Lookup VIRTUAL address in TLB
    - MISS → OS Trap
  - Lookup PHYSICAL address in INSTRUCTION CACHE
    - MISS → STALL waiting on MEMORY
  - Finally deliver instruction to INSTRUCTION REGISTER

Address Translation

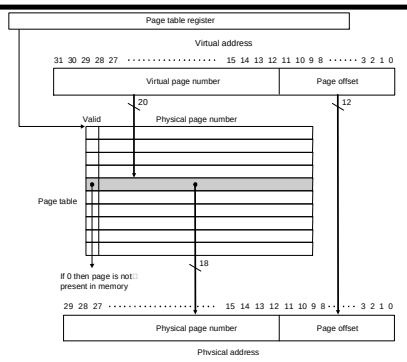
- Data Fetch
  - Use ALU to get VIRTUAL address
  - Lookup VIRTUAL address in TLB
    - MISS → OS Trap
  - Lookup PHYSICAL address in L1 DATA CACHE
    - MISS → STALL waiting on L2 DATA CACHE
  - Lookup PHYSICAL address in L2 DATA CACHE
    - MISS→ STALL waiting on memory
  - Finally Deliver data to the STALLED pipeline

Making Address Translation Fast

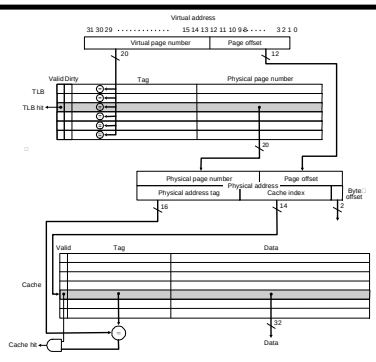


TLB = Translation Lookaside Buffer
a CACHE for address translation

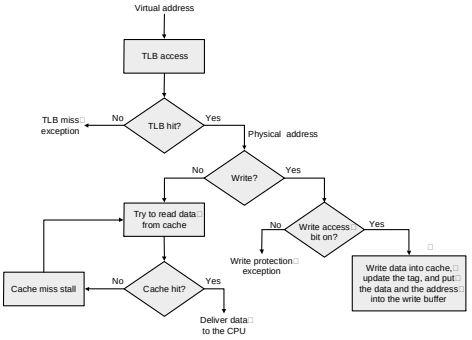
Virtual Address Translation



VM meets Cache



VM meets Cache



Classes to go

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