18 November

- 3 classes to go
- No class on Tuesday 23 November
- Last 2 classes will be survey and exam review
- Interconnect and IO

Goals of Interconnect

1. Modularity
   - Everything doesn't fit on a single chip (yet)
   - Where to draw the lines?
     - Minimize communication?
     - Minimize cost?
     - Maximize expandability?

2. Expansion
   - More processors
   - More memory
   - More devices

Backplane Bus

Issues in Interconnect

- Physical Interface
  - Single wire
  - Multiple wires
  - Radio
  - Light
- Protocol
  - Sync/Async
  - Master/Slave
  - Access Control
    - Time-Division Multiple Access
    - Frequency-Division Multiple Access
    - Code-Division Multiple Access

Ethernet
Magnetic Disk

Long term, nonvolatile storage
Large, inexpensive, and slow

Rotating platter(s) coated with magnetic material
Use a movable read/write head to access

Magnetic Disk Organization

- Cylinder: All tracks under head with arm in a fixed position
- Read/Write time has 3 components
  - Seek time to move the arm
  - Rotational latency: wait for the desired sector to come by
  - Transfer time: transfer bits

Typical Disk Times

- Average Seek: 8ms to 12ms
  - Sum of all possible seek / number of possible seeks
    - Locality reduces this to maybe only 25% of average number
- Rotational Latency:
  - At 5400 RPM → 11 ms
  - At 7200 RPM → 8 ms
  - At 10000 RPM → 6ms
- Transfer time depends on:
  - Transfer size (typical 512 bytes)
  - Rotation speed
  - Recording density
  - Diameter
  - Typical values: 10 to 30MBytes per second

USB

- Universal Serial Bus
- Provides power and signal
- A single host connects to multiple devices
- Devices are given 7 bit addresses when plugged in
  - Controller polls them round-robin
  - 1.5Mbit/s for USB 1, up to 486Mbit/s for USB 2.
  - Hot pluggable
  - Plug and Play

Firewire

- IEEE 1394
- Serial bus plus power
- Multiple masters
- Up to 800Mbit/s
- Hot pluggable
- Plug and Play

Interrupts

- How does the CPU manage SLOW I/O devices?
  1. Programmed I/O
  2. Interrupt Driven I/O
Polling

Advantages
Simple
No surprises
Processor in full control

Disadvantages
Polling can waste lots of time

Interrupt Driven I/O

Advantage
CPU only bothered when actually needed

Disadvantage
Can occur at surprising or inconvenient times
Have to save and restore state

MIPS Exceptions

- Reset
- Hardware Errors (Check, Bus Error, Cache Error)
- External Interrupt (6 inputs)
- Address Error
- Reserved Instruction
- TLB Miss
- System Call
- Breakpoint
- Trap
- Integer Overflow
- Floating Point Error
- Timer
- And a few more

Exception Processing

1. EPC gets address of faulty instruction or of next instruction depending on type of exception
2. Switch to kernel mode
3. Jump to a new location based on type of exception
   - PC ← FFFF FFFF BFC0 0000 for Reset
   - PC ← FFFF FFFF BFC0 0300 for Hardware error
   - PC ← FFFF FFFF BFC0 0380 for external interrupts
   - PC ← FFFF FFFF BFC0 0400 for ...
4. Save registers
5. Examine the ‘cause’ register to find out why you came here
6. Branch to code to do the right thing

Classes to go

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