February 13

- Test 1 Review
- Read the remainder of Chapter 3.

1

1. [5] A branch instruction changes the flow of control by (a) changing PC; (b) changing SP; (c) an address register; (d) none of the above.

Ordinary instructions increment the PC by 4 to determine the next instruction.

Branch instructions increment the PC by the offset in the immediate field changing the flow of control

2

2. [10] Consider a byte-addressable memory and an architecture that manipulates 4-byte words. What is the maximum number of words of memory available if the architecture has 13 bit addresses?

2^13 bytes / (2^2 bytes/word) = 2^11 words = 2048

3

3. [5] How many bits are in a megabyte?

2^20 bytes/megabyte * 2^3 bits/byte = 2^23 bits/megabyte
= 8 megabits = 8,388,608

4

4. [3] How many MIPS instructions fit in 32k bytes of memory?

$32 = 2^5$

$k = 2^{10}$

$32k = 2^5 * 2^{10} = 2^{15}$

MIPS instructions are 4 bytes = 2^2

$2^{15} / 2^2 = 2^{13}$ instructions = 8k = 8192

5

5. [12] Give as many different formulas as you can for execution time using the following variables. Each equation should be minimal; that is, it should not contain any variable that is not needed. CPI, R=clock rate, T=cycle time, M=MIPS, I=number of instructions in program, C=number of cycles in program.

(CPI * I * T)

(CPI * I / R)

(I / (M * 10^6))

(C * T)

(C / R)

(C / (CPI * M * 10^6))

6

6. [10] Consider the characteristics of two machines M1 and M2. M1 has a clock rate of 500Mhz. M2 has a clock rate of 600MHz. There are 4 classes of instructions (A-D) in the instruction set. In a set of benchmark programs, the frequency of each class of instructions is shown in the table.

Instruction Class	Frequency	M1 CPI	M2 CPI
A	40%	2	2
B	25%	3	2
C	25%	3	3
D	10%	5	4

What is the average CPI for each machine?

M1 = 0.4*2 + 0.25*3 + 0.25*3 + 0.1*5 = 2.8

M2 = 0.4*2 + 0.25*2 + 0.25*3 + 0.1*4 = 2.45

7

7. [10] How much faster is M2 than M1?

$(2.8 / 500) / (2.45 / 600) = 1.37$

37% faster.

8

8. [5] What is the cycle time of each machine?

M1 = 1/500MHz = 2ns = 2*10^-9 s

M2 = 1/600MHz = 1.67 ns = 1.67 * 10^-9 s

9

9. [10] If we make a low power version of M2 with a lower clock rate, what clock rate will we need to match the performance of M1?

$2.8 / 500 = 2.45 / X$

$X = 437.5$MHz

10

10. [15] You are going to enhance a machine, and there are two possible improvements: either make multiply instructions run 4 times faster than before, or make memory access instructions run 2 times faster than before. You repeatedly run a program that takes 100 seconds to execute. Of this time, 20% is used for multiplication, 50% for memory access instructions, and 30% for other tasks. What will be the speedup if you improve only multiplication? What will be the speedup if you improve only memory access? What will be the speedup if both improvements are made?

Speedup if we improve only multiplication = 100 / (30 + 50 + 20/4) = 100/85 = 1.18

Speedup if we only improve memory access = 100 / (30 + 50/2 + 20) = 100/75 = 1.33

Speedup if both improvements are made = 100 / (30 + 50/2 + 20/4) = 100/60 =1.67

11

11. [5] The pseudo instruction “move $t0, $t1” implements t0 = t1. Suggest an implementation using an actual instruction.

```
add     $t0, $t1, $zero
```

12

12. [3] How many bytes of memory are used by an array of 1000 pointers on the MIPS architecture?

1000 pointers * 32 bits/address / 8 bits/byte = 4000 bytes

13

13.[15] Add comments to each line and describe the function of the following code:

```
add     $t0, $a0,$a0    # t0 = 2*arg0
add     $t0, $t0, $t0   # t0 = 4*arg0
add     $t0, $t0, $a1   # t0 = arg1+4*arg0
lw      $t1, 0($t0)     # t1 = arg1[arg0]
addi    $t1, $t1, 1     # t1++
sw      $t1, 0($t0)     # arg1[arg0]=t1
```

Function is arg1[arg0]++

14

14. [5] What is the function of the SP register?

SP = stack pointer

Used to allocate and free storage on a LIFO basis as in function calls

15

15. [5] What is the function of the RA register?

RA = return address

Receives the address of the next instruction after a “jal” so we can return there after a function.

16

16. [10] Suppose I needed to determine the value of the PC at a particular point in a program. Give 2 different ways to get the value of PC into register $t0 using the instructions we have studied.

The load address “la” pseudo instruction with an instruction label as the argument would do it.

You could save RA, then jal to the next address, and move RA to t0, then restore RA.

Grade Distribution