29 March

- Problems with the exam...
- Problems with programs...
- Where we’re going from here.

Problems with Exam 2

- Question 4b was “premature”. I think maybe I mentioned locality but it was probably wrong to ask about it at this point.
- Question 5 unfortunately tested a detail instead of what I wanted. If it had said:

  > Suppose the target address “L1” for a beq instruction is 500k bytes away. This is too far away to represent in the 16 bit immediate address of the beq instruction. The “j” (jump) instruction *can* jump that far. What instruction sequence should we use to accomplish the goal of branching to L1 on equal compare without using any registers? (I’m interested in the idea here, not the exact instructions).

  It would have been more reasonable.
- Question 7 probably needed more time than was available.

In light of my errors, I’m going to reduce the “perfect score” threshold from 100 points to 90 points.

Problems with Programs

- Copying IS NOT ALLOWED! The POOP says:
  1. You are encouraged and expected to discuss the material in class and all assignments among yourselves.
  2. You are permitted to discuss all aspects of the assignments with anyone.
  4. You are encouraged and permitted to discuss and cooperate on all written assignments, but you are expected to understand all material that you submit.
  5. You are encouraged to discuss all programming assignments, but not your solutions. Specifically,
     a. To make learning to use the SPIM simulator easier, you are free to seek help from any source for the first two programming assignments. The programs you hand in must be your own work, but they can be based on unlimited help in all aspects from any sources whatsoever. You should cite in the documentation of your programs anyone who you worked with to complete your assignment.
     b. **The rest of the programs are to be done independently by each student.** For details on how the Honor Code applies to these programs, consult the handout 'Honor Code Observation in Computer Science Courses.'

Problems with Programs

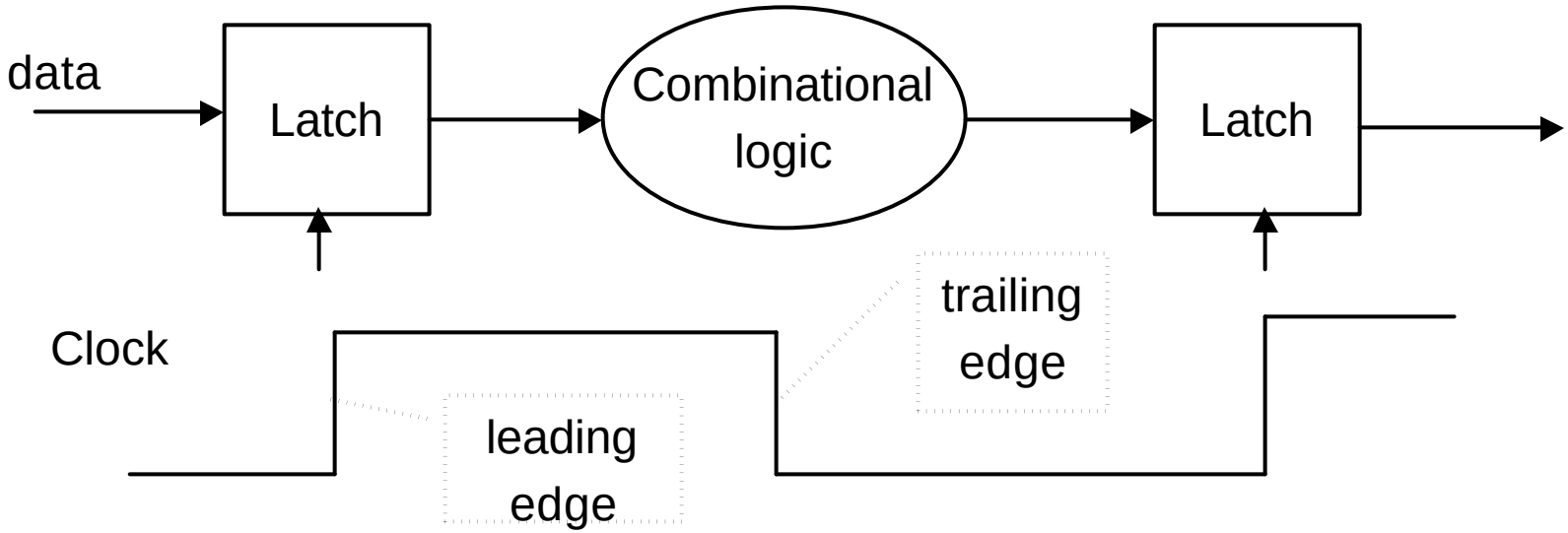
- THIS TIME, no action will be taken.

- NEXT TIME, we’re going to bust you.

9 Classes to GO!

- 4/3-5 Control/Sequencing
- 4/10-12 Cache memory
- 4/17-19 Virtual memory
- 4/24 System software
- 4/26 Course review
- 5/1 Exam review

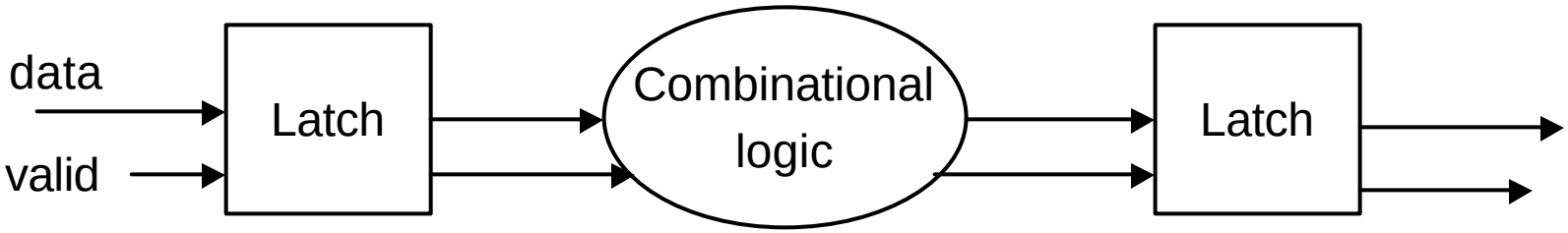
Synchronous Systems



On the leading edge of the clock, the input of a latch is transferred to the output and held.

We must be sure the combinational logic has *settled* before the next leading clock edge.

Asynchronous Systems



No clock!

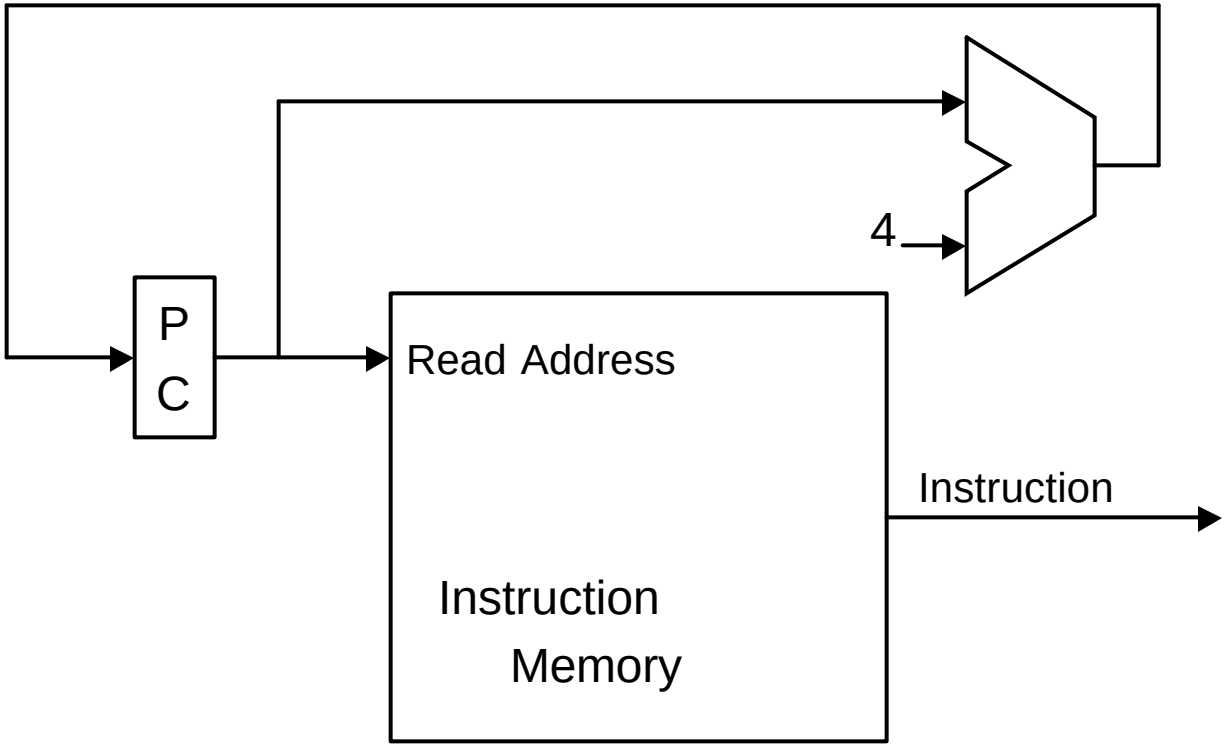
The data carries a “valid” signal along with it

System goes at greatest possible speed.

Only “computes” when necessary.

Everything we look at will be synchronous

Fetching Sequential Instructions



Datapath for R-type Instructions