

Quiz 1 Warm Up

- Format
 - Multiple choice
 - 25-30 questions
 - Open Book
 - Open Notes
 - No computers
 - No calculators



Sample Question #1

In a certain state automotive tags are assigned a unique ID composed of eight characters as follows: the first three characters are letters (A-Z), followed by a dash (-), and 4 decimal digits (0-9).

Q1) How many bits of information are in a tag as described above?

- (A) 8×8
- (B) $\log_2(26^3 10^4)$
- (C) $3 \times 5 + 1 + 4 \times 4$
- (D) $\log_2(256^8 / (26^3 10^4))$
- (E) none of the above

Sample Question #2

Q2) If you are told that the numeric part of the tag's ID (from the first question) is a palindrome (the same number forwards as backwards), how many bits of information are you given?

(A) 0

(B) 2×4

(C) $\log_2(26^3 10^2)$

(D) $\log_2((26^3 10^4) / (26^3 10^2))$

(E) none of the above

Sample Question #3

Q3) What hexadecimal number is equivalent to -33 in an 8-bit 2's complement representation?

(A) 0x21

(B) 0xA1

(C) 0xDE

(D) 0xDF

(E) none of the above

Sample Question #4

Q4) What is the most negative number representable in a 12-bit 2's complement binary number?

(A) -1024

(B) -2047

(C) -2048

(D) -4095

(E) -4096

Sample Question #5

There are 3 basic instruction formats in the MIPS instruction set architecture. They are:

R-type:	op	rs	rt	rd	shamt	funct
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I-type:	op	rs	rt	16-bit constant
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J-type:	op	26-bit constant
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- Q5) What aspect of the instruction's machine language encoding distinguishes between these different formats?
- (A) The presence or absence of an appropriately sized constant field in the instruction
 - (B) The number of register fields in the instruction
 - (C) The value of the opcode field
 - (D) Either appending an "i" to the end of a normal instruction or beginning the instruction with a "j"
 - (E) None of the above

Sample Question #6

Q6) Which of the following statements best describes the use of the `rt` field by the MIPS `sw` instruction.

- (A) The contents of the `rt` register are added to the signed 16-bit constant and used as a memory address
- (B) The contents of the `rt` register are added to 4 times the signed 16-bit immediate field and used as a memory address
- (C) The contents of `rt` are stored into memory
- (D) The contents of the memory location with the address pointed to by `rt` are stored in memory
- (E) The 5-bit value encoded in the `rt` field is stored in memory

Sample Question #7

Consider the following 5 MIPS instructions:

A:	lui	\$t1,4096
B:	la	\$t0,4096(\$t1)
C:	lw	\$t0,4096(\$t1)
D:	addi	\$t0,\$t1,4096
E:	sw	\$t0,4096(\$t0)

Q7) When executed in sequence, at what memory address (in hexadecimal) will the contents of \$t0 be stored by the instruction labeled E?

(A) 0x00001000

(B) 0x10001000

(C) 0x10002000

(D) 0x40964096

(E) The address cannot be determined from the instruction sequence alone

Sample Question #8

Consider the following 5 MIPS instructions:

A:	lui	\$t1,4096
B:	la	\$t0,4096(\$t1)
C:	lw	\$t0,4096(\$t1)
D:	addi	\$t0,\$t1,4096
E:	sw	\$t0,4096(\$t0)

Q8) Which two instructions perform identical operations?

- (A) Instructions labeled A and D
- (B) Instructions labeled B and C
- (C) Instructions labeled B and D
- (D) Instructions labeled B, C, and D
- (E) No two instructions are the same

Sample Question #9

Consider the following 5 MIPS instructions:

A:	lui	\$t1,4096
B:	la	\$t0,4096(\$t1)
C:	lw	\$t0,4096(\$t1)
D:	addi	\$t0,\$t1,4096
E:	sw	\$t0,4096(\$t0)

Q9) Which maximal set of instructions could be removed from the given sequence and have no effect on the results of the instruction labeled E?

- (A) The instructions labeled A and B
- (B) The instructions labeled B and C
- (C) The instructions labeled B, C, and D
- (D) The instructions labeled A, B, C, and D
- (E) None can be removed.

Sample Question #10

Consider the following “C” language code fragment:

```
if (a == 0) {  
    a = 1;  
} else {  
    a = 0;  
}
```

Q10) Which of the following MIPS instruction sequences performs the same operation as the given code fragment?

(A)

```
lw      $t0, a  
bne     $t0, $0, L1  
addi    $t0, $0, 1  
b       L2  
L1: add  $t0, $0, $0  
L2: sw   $t0, a
```

(B)

```
lw      $t0, a  
beq     $t0, $0, L1  
sw      $0, a  
b       L2  
L1: addi $t0, $0, 1  
sw      $t0, a  
L2:
```

(C)

```
lw      $t0, a  
sltiu   $t0, $t0, 1  
sw      $t0, a
```

(D)

```
lw      $t0, a  
addi    $t1, $0, 1  
beq     $t0, $0, L1  
addi    $t1, $0, 0  
L1: sw   $t1, a
```

(E) All of the above