A certain 32-bit, byte-addressable processor supports 128 Kbyte virtual memory page size. All page-table entries are stored in main memory. The results of these translations are cached in a 4-way set-associative translation look-aside buffer (TLB) with a total of 64 entries. On TLB misses a LRU replacement strategy is used. The next 5 questions refer to this processor.

1. Given a computer system with $2^{28}$ bytes of physical memory, how many bits of each page-table entry are needed to specify the physical page number?

2. Assuming that each page-table entry occupies 4 bytes, how many memory pages does the page table occupy?

3. What is the maximum size of a process’ working set that can achieve a 100% TLB hit rate? (that is after the initial compulsory misses)

4. Which of the virtual address bits would most likely be used to index a candidate set in the TLB cache?

5. How many bits are required for tag field of each TLB entry?