

Justin Heinecke - CV

Resume of Justin M Heinecke

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PRIMARY INTERESTS

Attached processors, computer graphics, digital audio and video capture, transport, processing.

QUALIFICATIONS

- SPI & i²c control; USB 2.0, TCP/IP
- Digital video (BT.656 et al) and audio (i²s)
- Synergy/RTL(Verilog)/Synopsys/Synplicity, Xilinx ISE & Vivado, Altera MaxPlus+II
- Gate Array ASIC & FPGA designs targeting multiple vendors
- Xilinx, Altera, Actel FPGA's and design systems
- Multi-FPGA implementations of ASIC designs
- Linux and Windows familiarity
- Code Composer Studio for TI DSP's; Visual Studio C++ for x86
- C, PASCAL, FORTRAN, COBOL, various assembly languages; also csh, awk, sed

EXPERIENCE SUMMARY

- Implemented all FPGA code for SD/HD audio/video capture products
- Architected a 4-channel AES/EBU audio capture daughter card, including schematics and full firmware support
- Designed, built, and wrote all programming for a floating-point accelerator boardset
- Synthesis, simulation, layout, place & route for full custom and sea-of-gates ASICS
- Intimate hardware bringup experience, including scopes, analyzers, and surface mount rework
- Wrote numerous Visual 'C/C++' gui suites for bringup and debug
- Wrote Unix kernel and driver enhancements to support new products
- 'C' - more than 30 years experience
- 'Verilog' - more than 20 years experience

RELEVANT EXPERIENCE

Consultant – Hardware Engineer 9/98-current

Various clients including Rambus Inc and Western Digital. Positions involved both 1099 contracts and staffing agency (W2) placements.

- ***Black Forest Engineering (Triple Crown) 5/18-current (intermittent)***
Colorado Springs, CO (hybrid)

Assisted with design of a custom FPGA-based image processing board (Xilinx, Artix-7, Vivado) and ported an ASIC image processing design into the FPGA. Overhauled and enhanced the design, including in-house developed local & global histogram equalization & scaling algorithms (developed with Octave (a Matlab alternative)), i²c and spi controllers, conversion from a parallel flash to a serial flash, and design-for-test improvements. Performed synthesis and timing closure and developed a massive simulation suite, and then ported the FPGA design back into an ASIC. Built a control gui using Opal-Kelly USB interface in Visual C++. Developed a suite of scripts (sed, awk, perl) for manipulating and uploading images into dram & flash, and into Vivado.

Clean-up and enhancements to firmware of Opal-Kelly based USB interface boards, and porting from Spartan-6/ISE to Spartan-7/Vivado.

- ***Aperi (Oxford International) 1/17-6/17***
Camarillo, CA (remote)

Developed FPGA code for TCP/IP packet classification and translation in a Video Over IP switching network product (Xilinx Kintex-7, Vivado) including a massive macro-configurable pattern-matching block, and built a tcp/ip control gui in Visual C++.

- ***Freelance design 1/14-current***
Chapel Hill, NC

Developed a variety of small projects based on Atmel, Microchip, and Freescale microcontrollers; completed Google's Android Development course & working on an Android app; startup of a sole

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proprietorship to produce and sell high quality fractal artwork.

- **Aqueti / AQT 9/15-10/15**

Durham, NC

Consulted on establishing FPGA architectures for portable J2K video compression and for X-ray scattering analysis. (Altera, Xilinx)

- **Egonocast 3/13-11/13**

Paris, France (remote)

Designed and prototyped a USB audio capture device to acquire 3 AES/EBU audio pairs at 48kHz. Wrote all FPGA code for capture, mixing, and downsampling, and uploading (Spartan6, Cypress FX2-LP) and adapted a Windows driver reference design to read all four endpoints asynchronously. Also wrote a host gui to initiate, save, and verify all captured data and created a data generator module to produce 3 AES/EBU audio pairs (Xilinx Spartan-3, ISE).

- **SmallHD 6/13-8/13 (1099)**

Cary, NC

Diagnosis/repair of existing FPGA code to eliminate stubborn glitches in an SDI/HD-SDI and analog video capture and display device; added an edge-enhancement feature to the display; set up a host-based debug capability. (Lattice FPGA)

- **Western Digital 4/12-6/12 (Oxford International)**

Longmont, CO

Serialized a set of ARM AXI busses to efficiently span a multi-FPGA partition (macro configurable to use anywhere from 3 wires to over 500 wires); converted a SDR SAS/SATA channel to DDR using Xilinx GTX and serdes blocks. (Xilinx Virtex-6, Cadence NC-Verilog/System Verilog)

- **Viewcast 9/98-6/12 (intermittent) (1099)**

Morrisville, NC; Dallas, TX

Sole responsibility for all FPGA (Xilinx Spartan 3, ISE) code for a DSP based (TI TMS320DM642) SDI/HD-SDI video transceiver PCI-ex card, including system architecture, synthesis, simulation and verification, and static timing analysis, as well as hardware bringup and verification, both standalone and within a Windows environment. Architected a 4-channel AES/EBU capture daughter card, including schematics and full firmware support. Developed a Windows based i²c control suite gui for full system verification. Work included two generations of unreleased PCI and PCI-ex products.

Worked with a team to complete an FPGA (Altera) based audio/video capture PCI card, concentrating primarily on Verilog synthesis and simulation, and taking on full responsibility for embedded firmware (Keil runtime environment) and FPGA code for an IEEE-1394 digital video daughterboard (Altera, Philips P89C51, Divio NW701). Also included architectural design work and surface mount prototyping.

Hewlett-Packard Co. 5/96-2/98

Chapel Hill, NC

VLSI Design Engineer

Brought a rough schematic outline into Verilog; through system verification and logic synthesis with Cadence Synergy; compiled into standard cells with Oasis; and laid out the chip with Magic. This three million transistor design, a mixture of standard cell and full custom, is the Geometry Network Interface for the Pixel Flow graphics machine started at the University of North Carolina at Chapel Hill and developed by Hewlett-Packard (never released.)

Sun Microsystems, Inc. 10/87-10/94

Research Triangle Park, NC

Member of Technical Staff - Hardware Engineer

Brought a rough hierarchical Verilog ASIC design for an ATM store-and-forward device through full system verification, managed the logic synthesis with Synopsys through multiple iterations to achieve design timing requirements, and moved the design and the Verilog test vectors into the vendor's toolsets (TI) and to tapeout

Laid out the basic architecture, floor plan, and pinout of a ~72000 cell ASIC, a major part of a real-time MPEG video encoder board, established the Synopsys hierarchical synthesis methods to achieve conflicting gate count and timing requirements, and moved the design into the vendor's toolset (LSI).

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Designed the system controller FPGA (Actel) for a 4-processor graphics accelerator incorporating the Intel i860 RISC processor (embedded Unix derivative), established the diagnostics strategy including directing the diagnostics efforts of two other engineers, and participated in hardware bringup and the transfer of the design from engineering to manufacturing and through to First Customer Ship.

Implemented all diagnostics for a 2 board VLIW bit-slice graphics/applications accelerator based on the AMD 2910 sequencer and played a key role in subsequent bringup of the entire system.

Adage, Inc. 4/86-5/87

Raleigh, NC

Software Engineer

Developed software to connect Micro-VAX hardware to a custom 5080 emulator, working with DEC engineers to develop a custom driver, and wrote all the system messaging software.

University of North Carolina 9/83-9/85

Chapel Hill, NC

Graduate Assistant – Computer Science Department

Designed a floating-point accelerator for the Pixel-Planes 4 project at the Micro Systems Laboratory, using the AMD 2910 for the processing pipeline; developed its assembler, simulator, and netlister; and oversaw floorplanning and hardware construction.

Applied Dynamics International 11/80-5/82

Ann Arbor, MI

Software Engineer

Took over development of the prom-based operating system for an NTSC raster graphics system based on the TMS-9900 processor, developing an overlay mechanism to extend the effective prom capacity, and developed extension firmware for an AMD 2910-based graphics accelerator and a full color RGB frame buffer.

Other relevant work

Designed and built an iPod controller board, including software (Atmel ATtiny13), schematics and board layout (Eagle).

Modified a NetBurner design (Freescale) to look up an IP address from a URL, and to specify the IP port for the embedded configuration web server, part of an IP-addressable X10 controller.

Wrote a Windows program to generate high resolution fractal images (C++, MFC) (see fractalsbyjustin.com).

Wrote an Android app to display ham radio frequency and mode over Bluetooth from ICOM transceivers.

Education

- BA Physics and Mathematics, Valparaiso University – 5/77
- BS Electrical Engineering, Valparaiso University – 5/77
- MS Computer Science, University of North Carolina - Chapel Hill – 5/85

Technical Skills and other Qualifications

- IEEE Senior Member 2015
- Amateur Radio Extra Class Operator – KD4CPM
- Member, Tau Beta Pi (EE Honor Society), Sigma Pi Sigma (Physics Honor Society)

Other Accomplishments

Three solo coast-to-coast bicycle tours (6-8/76, 6-9/80, 6-10/87)