Multiwire Differential Signaling

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Version 1.1

1. Overview

This document describes and discloses a set of ideas for improving the bandwidth on a signaling system composed of more than one wire. These ideas represent a generalization of practiced 2-wire differential signaling, widely used in computer and communications systems. The central notion is to group a set of N wires together (N > 2), allowing more than one symbol to be transmitted on the wire-set per symbol time; the signal levels on the set of wires are adjusted so that (1) the currents in the wires sum to zero and (2) there is always a voltage difference between all pairs of wires in the set.

2. Background

2.1 Differential Signaling

Differential signaling is commonly used in high-performance communications systems. The basic elements of a differential signaling system are shown in Figure 2.1.

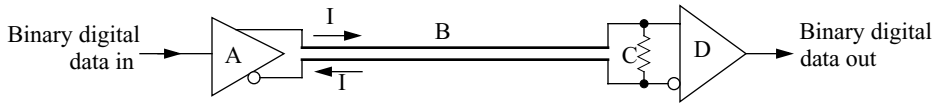


Figure 2.1. A differential signaling system.

These elements include:

1. A transmitter (A) that converts a stream of binary digital data bits on its input (usually represented as two voltage levels) into a pair of equal and opposite currents (or voltages) at its outputs. The current (voltage) outputs represent a simple encoding of the input bits, for example, with I = +i representing a logical “1” and I = –i representing a logical “0”. The two states (I = +i,–i) represent two possible *symbols* corresponding to digital “0” and “1”.
2. A transmission line (B) transports the differential current (voltage) signal from transmitter to receiver. A transmission line in a differential signaling system usually consists of a pair of identical, closely-coupled wires or conductors that form a coupled 2-conductor transmission line.
3. A terminator (C) absorbs signaling symbols (changes in I) as they arrive at the receiver end of the transmission line, thus preventing reflections of the symbols back into the line where they might interfere with symbols transmitted at a later time. If the symbols are represented as currents, the terminator, typically a resistor, converts the signal current to a voltage across the

receiver inputs. Often an additional terminator is provided at the transmitter; the purpose of a transmitter terminator is to absorb reflections from any discontinuities in the transmission line between transmitter and receiver.

4. A receiver (D) compares the voltages at the two ends of the terminator and converts this voltage difference back into binary digital bits, typically represented as two voltage levels.

Differential signaling has several advantages over *single-ended* signaling:

1. In single-ended signaling, binary digits are (typically) represented as two different voltage (or current) levels on a single wire; the receiver must have a built-in or external reference voltage (current) to compare the signal against in order to recover the data. In differential signaling, no reference is required since there is inherently a voltage difference to detect.
2. If the wires that make up the transmission line are closely spaced and of the same length, composition, and geometry, then any noise injected into the signaling system is injected equally into the two lines and appears as a *common-mode* signal at the receiver. It is easy to construct differential receivers that have very low common-mode gain and very high differential gain, and thus a high *common-mode rejection ratio*, the ratio of the differential gain to the common-mode gain. Since most sources of noise in a differential signaling system are common-mode, such signaling systems reject noise inherently.
3. The signal at one end of the terminator (D) in a differential signaling system swings between +V and −V, while the voltage at the other end of the terminator swings between −V and +V. Thus the receiver sees a voltage difference of 2•V between the two symbols. The two-wire signaling system in essence doubles the signal available for detection at the receiver.
4. Since a differential signaling system requires no reference, provides a receiver voltage of twice the signal swing, and inherently rejects most sources of noise, very small signal levels may be employed, allowing the signaling system to consume relatively little power.

2.2 Enhancements to Differential Signaling

The main disadvantage of differential signaling as opposed to single-ended signaling is that two wires are required to carry symbols from transmitter to receiver, rather than one. In a simple encoding scheme, where the two possible symbols encode a binary digit (bit), the efficiency of a differential signaling system is exactly 0.5 bit/wire. This efficiency may be improved if a signaling system consists of several parallel channels. One such method is outlined in Figure 2.2.

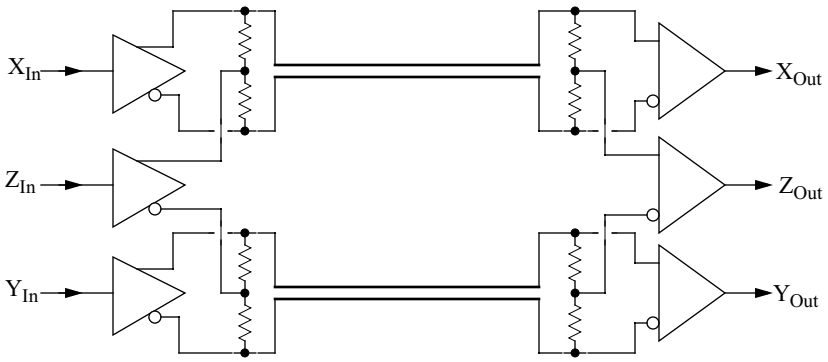


Figure 2.2. Improving signaling efficiency with a “phantom” line.

Channels “X” and “Y” are conventional differential signaling channels. Each is equipped with center-tapped terminators at both transmitter and receiver. The center taps in no way affect the operation of the “X” and “Y” channels, and in the absence of the “Z” circuitry, the center taps of all terminations resistors would be at a fixed voltage (assuming perfectly balanced voltages/ currents out of the transmitters), namely the common-mode voltage, Vcm, of the signaling system. The “Z” channels transmitter establishes a voltage difference between Vcm on the “X” channel and Vcm on the “Y” channel. This voltage difference propagates down the two transmission lines of the “X” and “Y” channels and creates a voltage difference between the center taps of the receiver terminators on the “X” and “Y” receivers. This difference is detected by the “Z” receiver which recovers the “Z” bit stream. In this improvement, the effeciency of the signaling system is increased for 0.5 to 0.75, since 3 bits can be transmitted per symbol on 4 wires.

This method of piggy-backing a third channel onto two conventional differential channels is referred to as a “phantom”, and has been routinely practiced in wired telephony for many decades [1].

The “phantom” idea can be extended to a collection of four differential channels, with phantoms, to allow the addition of a 7th channel, as shown in Figure 2.3.

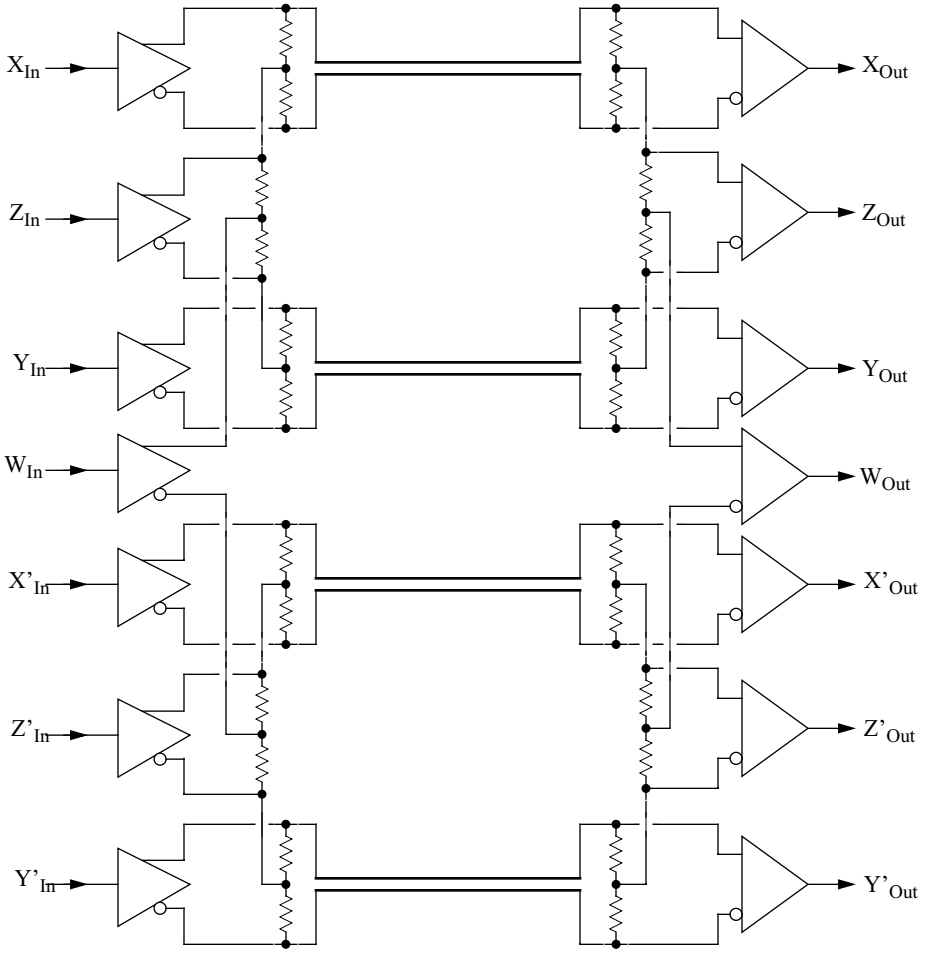


Figure 2.3. A “ghost” channel.

Channels X,Y and X',Y' comprise two sets of two conventional differential channels, each with phantom channels Z,Z'. A seventh channel, "W", can be added by differentially driving the common-mode voltages of the two phantoms. "W" is referred to in telephony as a "ghost" channel. The efficiency of a "ghost" arrangement is 7/8.

Yet another level of hierarchy is sometimes added, a "wraith" channel, by carrying this idea one step further; we will not attempt to draw this configuration. The efficiency of the "wraith" arrangement is 15/16, very nearly one bit per symbol per wire, the efficiency of a conventional single ended system.

In computer communications systems, the phantom/ghost/wraith idea cannot be carried far in practice because the absolute value of the signals at a given receiver may be driven outside the *common-mode range*, the allowable range of voltage on input terminals of the receiver. In practical receivers, this range is almost always restricted to within the power supply voltages, and often much less.

2.3 Multilevel Signaling

It is possible to improve the efficiency of any signaling system by sending more than one bit per symbol. This requires the definition of more than two symbols, or, in other words, more than two signal levels. Suppose, for example, that a signaling system has three possible symbols +V, 0, and −V, then it is possible to encode 1.5 bits/symbol for an effeciency of 1.5 on a single-ended system or 0.75 on a differential system.

Multi-level signaling requires a more complex reference, however, than a conventional two-level signaling scheme. For three levels, two references are required, ideally placed at +V/2 and −V/2. There is little advantage to transmitting three-level signaling differentially, though is is possible to recover the advantage of noise cancellation in a multi-level differential signaling scheme when the number of levels is even (4,6,8...). An N-level differential signaling system (N even) requires N-1 reference voltages.

It should be noted that engineering a stable reference is quite difficult. Usually, the need for a reference increases the required signaling voltage (current) levels, and multiple references exacerbate the problem.

3. Multiwire Differential Signaling

We introduce a (so far as we know) new method that extends and generalizes conventional 2-wire differential signaling, supports multi-level signaling, greatly increases signaling effeciency, but retains essentially all of the advantages of the conventional 2-wire scheme. Like "phantom" channels, multiwire differential signaling employs groups of N wires (N > 2) to improve efficiency. Multiple signal levels (>2) are used to further improve efficiency, but like conventional 2-wire differential signaling, our form of multi-level signaling requires no receiver reference. We introduce this idea with two examples, (N=3 and N=4) then briefly develop some general properties of arbitrary N-wire systems.

3.1 3-Wire Differential Signaling

Consider a signaling system with three wires. These are driven differentially by three transmitter, which, for purposes of this discussion are current transmitter (voltage transmitters will

work as well, with appropriate modification). The receiver likewise consists of three differential elemental receivers. The arrangement is shown in Figure 3.1.

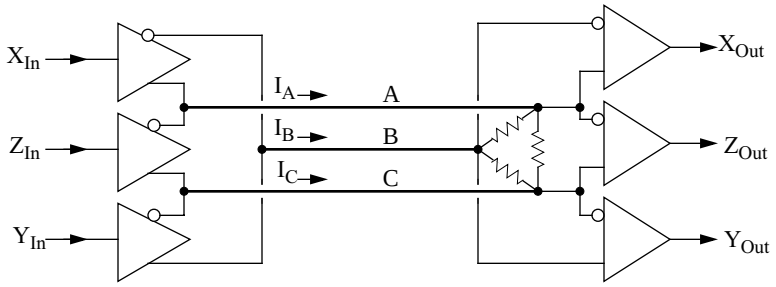


Figure 3.1. 3-wire differential signaling.

The transmitters are conventional differential ones; for purposes of this example, we will assume that they are current transmitters, that is, the binary value on the transmitter input is converted to a differential current, with "1" corresponding to $I_{Out} = +i$ and "0" to $I_{Out} = -i$. Specifically, I_{Out} is the current driven onto the non-inverting output port and the negative of that current is driven onto the inverting output; the sum of these currents is always 0. The method will work equally well with transmitters that output two voltage levels, but a means must be provided for summing the voltages onto the three wires, for example a resistor network. The receivers are conventional differential receivers, which convert a voltage difference to a binary digital value.

As in conventional 2-wire differential signaling, we require two constraints on the signal currents I_A, I_B, and I_C injected into the three wires (A,B,C) of the transmission line for all allowed symbols:

1. The sum of the currents must be zero ($I_A + I_B + I_C = 0$); this is guaranteed to be true for differntial current transmitters.
2. The voltage difference at each pair of receiver terminals must be non-zero; this is not guaranteed to be true for all possible values on X_{In},Y_{In},Z_{In}.

We can find the signal voltages at the three receivers by solving Kirchoff's loop and nodal equations for the currents and voltages at the terminator (Figure 3.2).

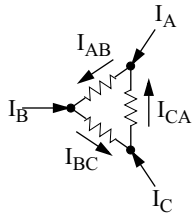


Figure 3.2. Currents in 3-wire terminator.

The nodal equations are

Eq 3. 1
$$I_A = I_{AB} - I_{CA}$$
$$I_B = I_{BC} - I_{AB}$$
$$I_{AC} = I_{CA} - I_{BC}$$

The voltages at the receivers are

Eq 3. 2
$$V_{AB} = I_{AB}R$$
$$V_{BC} = I_{BC}R$$
$$V_{CA} = I_{CA}R$$

The loop equation says that the sum of the receiver voltages is = 0, so

Eq 3. 3 $$I_{AB} + I_{BC} + I_{CA} = 0$$

Adding the first of Eq 3. 1 to minus the second, we have

Eq 3. 4 $$2I_{AB} = I_A - I_B + I_{BC} + I_{CA}$$

But from Eq 3. 3, $I_{BC} + I_{CA} = - I_{AB}$, so $V_{AB} = 1/3 \bullet R(I_A - I_B)$. So, the receiver voltages are:

Eq 3. 5
$$V_{AB} = 1/3 \cdot R(I_A - I_B)$$
$$V_{BC} = 1/3 \cdot R(I_B - I_C)$$
$$V_{CA} = 1/3 \cdot R(I_C - I_A)$$

From these equations, we see that the second constraint is satisfied only if all three currents are different. Table 3.1 lists the allowable values of current on the three wires that satisfy these contraints, consistent with differential current transmitters. The voltages presented to the three differential receivers and the binary digital values on the channels X, Y, and Z that correspond to these current values are also listed, where V = iR.

Table 3.1 : Allowed currents and corresponding bit values for 3-wire differential signaling.

I_A	I_B	I_C	V_{A-B}	V_{B-C}	V_{C-A}	X	Y	Z
-2i	0	+2i	-2/3V	-2/3V	+4/3V	0	0	1
0	+2i	-2i	-2/3V	+4/3V	-2/3V	0	1	0
-2i	+2i	0	-4/3V	+2/3V	+2/3V	0	1	1

Table 3.1 : Allowed currents and corresponding bit values for 3-wire differential signaling.

I_A	I_B	I_C	V_{A-B}	V_{B-C}	V_{C-A}	X	Y	Z
+2i	-2i	0	+4/3V	-2/3V	-2/3V	1	0	0
0	-2i	+2i	+2/3V	-4/3V	+2/3V	1	0	1
+2i	0	-2i	+2/3V	+2/3V	-4/3V	1	1	0

Several points can be drawn from this table of allowable current values and corresponding binary digital values:

1. There are six possible symbols that satisfy the two constraints on the signaling currents; they are the current combinations in which no two line currents are equal.
2. Each receiver sees one of four values of differential signal (+4/3•V,+2/3•V,–2/3•V,–4/3•V), V=iR.
3. The six symbols represent 6 out of a possible 8 encodings of 3 binary digits; states X,Y,Z = 000 and 111 are disallowed, since they would result in no differential voltages across any of the pairs.

A 3-wire signaling system contructed in this way retains essentially all of the useful properties of conventional 2-wire differential signaling:

1. No receiver reference is required, since all symbols produce a unique set of voltage differences at the three receiver terminals.
2. If the 3 wires that make up the transmission line are identical in composition closely coupled any noise injected into the signaling system is common-mode to the three receivers, and is rejected by the common-mode ratio of the receivers.
3. The 3-wire arrangement preserves the low-voltage, low-power properties of 2-wire differential signaling.

The efficiency of a 3-wire system is computed as follows: during each symbol time a symbol can be transmitted that represents 1 of 6 possible values, thus representing $\log_2(6)$~2.5 bits/symbol. Efficiency is therefore 2.5/3 = 0.83 bits/symbol/wire, about a 67% improvement over conventional differential signaling. Power consumed in a 3-wire system is exactly 3x the power of a 2-wire system, so the improved efficiency is fairly expensive in terms of power consumption.

To make practical use of an 3-wire differential signaling system requires converting conventional multi-bit binary data into a set of base-6 symbols. $6^4 = 1296$ is the smallest power of 6 that is larger than $2^8 = 256$, so at least 4 symbols are requied to send a byte (8 bits) of data. These four symbols can either be sent sequentially, on four subsequent bit-clock cycles on a single 3-wire system, or simultaneously on a single bit-clock cycle on four parallel 3-wire channels. The state space for 6^4 is much larger than necessary to send a byte; the excess state space could be used to transmit the parity of the data word, to ensure sufficient transitions on the data wires for clock recovery, to DC balance the signaling system, or to send out-of-band control characters interspersed with data. Coding for multi-wire signaling systems is discussed in more detail in Section 3.4.

3.2 4-Wire Signaling Systems

A four-wire scheme is outlined in Figure 3.3.

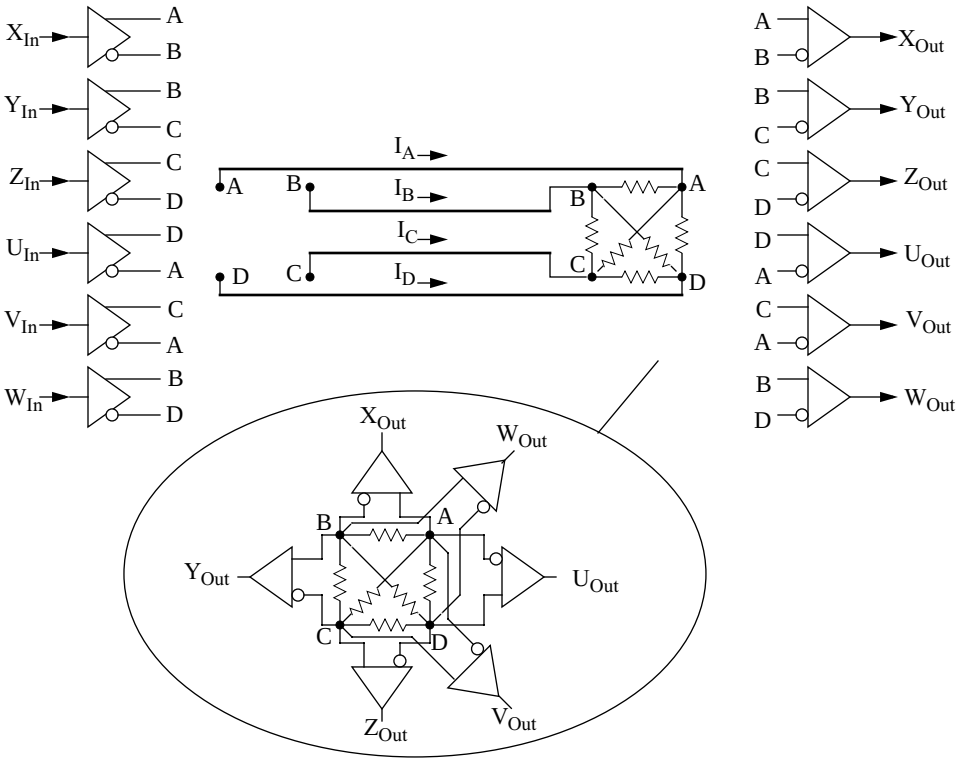


Figure 3.3. 4-wire differential signaling.

Six transmitters drive the six possible pairings of four wires, and the data is recovered at six differential receivers. It is difficult to draw the connections clearly; the inset is intended to make the connections somewhat clearer.

We can find the signal voltages at the six receivers as in the 3-wire case by solving Kirchoff's loop and nodal equations for the currents and voltages at the terminator (Figure 3.4).

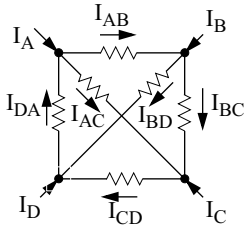


Figure 3.4. Currents in 4-wire terminator.

The nodal equations are

$$
\begin{aligned}
I_A &= I_{AB} + I_{AC} - I_{DA} \\
I_B &= -I_{AB} + I_{BC} + I_{BD} \\
I_C &= -I_{BC} + I_{CD} - I_{AC} \\
I_D &= -I_{CD} + I_{DA} - I_{BD}
\end{aligned}
\qquad \text{Eq 3. 6}
$$

The voltages at the receivers are $V_{AB} = I_{AB}R$, etc. There are four voltage loops in the circuit, and the four loop equations are

$$
\begin{aligned}
V_{AB} + V_{BD} + V_{DA} &= 0 \\
V_{AB} + V_{BC} + V_{CA} &= 0 \\
-V_{CA} + V_{CD} + V_{DA} &= 0 \\
V_{BC} + V_{CD} - V_{BD} &= 0
\end{aligned}
\qquad \text{Eq 3. 7}
$$

from which we can write the four equivalent relations for the currents

$$
\begin{aligned}
I_{AB} + I_{BD} + I_{DA} &= 0 \\
I_{AB} + I_{BC} - I_{AC} &= 0 \\
I_{AC} + I_{CD} + I_{DA} &= 0 \\
I_{BC} + I_{CD} - I_{BD} &= 0
\end{aligned}
\qquad \text{Eq 3. 8}
$$

From the Eq 3. 6, Eq 3. 7 and Eq 3. 8, we can find the voltages; all are of the form

$$V_{AB} = 1/4 \cdot R(I_A - I_B) \qquad \text{Eq 3. 9}$$

As in the 3-wire case the receiver-voltage constraint is satisfied only if all four currents are different. For the 6 input bits X,Y,Z,U,V,W, there are 64 possible combinations of currents. All but 24 fail to satisfy this requirement, and lead to zero voltage across one or more of the receivers.

Table 3.2 lists the allowable values of current on the 4 wires that satisfy the multi-wire signaling constraints. The voltages presented to the 6 differential receivers and the binary digital values on the channels X, Y, Z, U, V, W that correspond to these current values are also listed; here V = iR.

Table 3.2 : Allowed currents and corresponding bit values for 4-wire differential signaling.

I_A	I_B	I_C	I_D	V_{A-B}	V_{B-C}	V_{C-D}	V_{D-A}	V_{C-A}	V_{B-D}	X	Y	Z	U	V	W
-3i	-i	+i	+3i	-1/2V	-1/2V	-1/2V	+3/2V	+V	-V	0	0	0	1	1	0
-i	+i	+3i	-3i	-1/2V	-1/2V	+3/2V	-1/2V	+V	+V	0	0	1	0	1	1
-3i	-i	+3i	+i	-1/2V	-V	+1/2V	+V	+3/2V	-1/2V	0	0	1	1	1	0
-3i	+i	+3i	-i	-V	-1/2V	+V	+1/2V	+3/2V	+1/2V	0	0	1	1	1	1
+i	+3i	-3i	-i	-1/2V	+3/2V	-1/2V	-1/2V	-V	+V	0	1	0	0	0	1
-3i	+i	-i	+3i	-V	+1/2V	-V	+3/2V	+1/2V	-1/2V	0	1	0	1	1	0
-3i	+3i	-i	+i	-3/2V	+V	-1/2V	+V	+1/2V	+1/2V	0	1	0	1	1	1

Table 3.2 : Allowed currents and corresponding bit values for 4-wire differential signaling.

I_A	I_B	I_C	I_D	V_{A-B}	V_{B-C}	V_{C-D}	V_{D-A}	V_{C-A}	V_{B-D}	X	Y	Z	U	V	W
-i	+i	-3i	+3i	-1/2V	+V	-3/2V	+V	-1/2V	-1/2V	0	1	0	1	0	0
-i	+3i	-3i	+i	-V	+3/2V	-V	+1/2V	-1/2V	+1/2V	0	1	0	1	0	1
-i	+3i	+i	-3i	-V	+1/2V	+V	-1/2V	+1/2V	+3/2V	0	1	1	0	1	1
+i	+3i	-i	-3i	-1/2V	+V	+1/2V	-V	-1/2V	+3/2V	0	1	1	0	0	1
-3i	+3i	+i	-i	-3/2V	+1/2V	+1/2V	+1/2V	+V	+V	0	1	1	1	1	1
+3i	-3i	-i	+i	+3/2V	-1/2V	-1/2V	-1/2V	-V	-V	1	0	0	0	0	0
-i	-3i	+i	+3i	+1/2V	-V	-1/2V	+V	+1/2V	-3/2V	1	0	0	1	1	0
+i	-3i	-i	+3i	+V	-1/2V	-V	+1/2V	-1/2V	-3/2V	1	0	0	1	0	0
+i	-3i	+3i	-i	+V	-3/2V	+V	-1/2V	+1/2V	-1/2V	1	0	1	0	1	0
+i	-i	+3i	-3i	+1/2V	-V	+3/2V	-V	+1/2V	+1/2V	1	0	1	0	1	1
+3i	-3i	+i	-i	+3/2V	-V	+1/2V	-V	-1/2V	-1/2V	1	0	1	0	0	0
+3i	-i	+i	-3i	+V	-1/2V	+V	-3/2V	-1/2V	+1/2V	1	0	1	0	0	1
-i	-3i	+3i	+i	+1/2V	-3/2V	+1/2V	+1/2V	+V	-V	1	0	1	1	1	0
+3i	-i	-3i	+i	+V	+1/2V	-V	-1/2V	-3/2V	-1/2V	1	1	0	0	0	0
+3i	+i	-3i	-i	+1/2V	+V	-1/2V	-V	-3/2V	+1/2V	1	1	0	0	0	1
+i	-i	-3i	+3i	+1/2V	+1/2V	-3/2V	+1/2V	-V	-V	1	1	0	1	0	0
+3i	+i	-i	-3i	+1/2V	+1/2V	+1/2V	-3/2V	-V	+V	1	1	1	0	0	1

Several points can be drawn from this table of allowable current values and corresponding binary digital values:

1. There are 24 possible symbols that satisfy the two constraints on the signaling currents.
2. Each receiver sees one of 6 values of differential signal (+3/2•V,+V,+1/2•V,-1/2•V,-V,-3/2•V), with V=iR.

The state-space for 4-wire differential signaling is 24, so a given symbol can encode $\log_2(24)$ = 4.585 bits, for an efficiency of 1.146 bits/symbol/wire, slightly better than the efficiency of a conventional single-wire signaling system.

A practical 4-wire differential signaling system requires conversion of multi-bit binary data to the 1-of-24 form required in the signaling system. $24^2 = 576$, which can encode, for example, 8 bits together with a 9th parity bit (512 states), wthe 576-512 = 64 states left over for encoding out-of-band control codes and the like. See Section 3.4 for additional details on coding.

3.3 General Properties of N-wire Signaling Systems

As outlined above, all N-wire signaling systems must obey the two constraints:

1. The sum of the currents must be zero ($\sum_{0}^{N} I_j = 0$).
2. The voltage difference between any pair of receiver terminals must be non-zero.

Since there are receivers across all pairs of wires, (2.) implies that all wires must carry different currents. Each wire can carry up to a maximum of ±(N-1)•i, since there are N-1 transmitter terminals attached to each transmission line wire. As we have seen for the two specific cases (N=3 and N=4), the allowed values, ones that provide distinctly different currents on each wire,

range from -(N-1)•i up to +(N-1)•i in steps of 2•i, so there are N distinct signal levels. The valid symbols are permutations of these voltages, so, there will be **P**(N) = N! possible states, or N! symbols on an N-wire signaling system. The bit efficiency of an N-wire system is ($\log_2$(N!)/N bits/symbol/wire. The number of transmitters (and receivers) required is found by computing N things taken 2 at a time (N-choose-2),

Eq 3. 10 $$C(N, 2) = P(N, 2)/2! = N!/2(N-2)!$$

These parameters for N-wire systems are listed for various values of N below in Table 3.3.

Table 3.3 : # Symbols and Efficiency for N-wire Differential Signaling

N (# wires)	N!/(2•(N-2)!) (# tx,rx)	N! (# symbols)	Efficiency (bits/symbol/wire)
2	1	2	0.5
3	3	6	0.8617
4	6	24	1.1462
5	10	120	1.3814
6	15	720	1.5820
7	21	5,040	1.7570
8	28	40,320	1.9124
9	36	362,880	2.0521
10	45	3,628,800	2.1791

Note that, as N increases, the power required to deliver a given amount of bandwidth increases faster than would the power for a group of conventional 2-wire differential channels with roughly the same bandwidth. An N-wire signaling system's power increases as the number of transmitters (second column in the table). For a 4-wire system, for example, power is $6i^2R$ (i is the signal current out of one transmitter and R is the termination resistance); such a system delivers about 4.5 bits/symbol on four wires. 4.5 2-wire channels would be required to deliver the same bandwidth, and they would consume $4.5i^2R$, so power is about 30% higher in the multi-wire differential signaling system, for N=4. However, the strength of the method is in conserving wires and pins, not necessarily power.

Also note that as N increases, the number of discrete signal levels = N, and the number of possible differential voltages across any given pair receiver input terminals is the same as the number of receivers (transmitters), N!/(2•(N-2)!). It is not clear that it is practical to extend the method beyond N=4-6, as the complexity of the transmitter, data coding, and the maximum voltage swing on a receiver input rapidly become prohibitive.

3.4 Coding on Multiwire Signaling Systems

In order for multiwire differential signaling to be useful, we require an effective means of encoding binary data for transmission over an N-wire signalling system. We introduce the term *symbol number* to refer to a binary-encoded number denoting one of the base-N symbols suitable for transmission over an N-wire differential signaling system. Symbol numbers for an N-wire system will be $M=\log_2(N!)$ bit binary numbers that take on values in the range 0..N!. We express these binary symbol numbers as b{M..0}. We first consider the problem of encoding symbol numbers into their corresponding drive words needed to feed the transmitters. Recall that an N-wire line has L = C(N,2) (N-choose-2) transmitters, so the drive words will be L bits wide.

Note that any invertible mapping from symbol numbers into valid transmitter drive words can be used. The general technique is to start with a table that enumerates all of the valid drive words, assign symbol numbers to those drive words in order, and then permute the mapping so that the digital logic required to map M-bit symbol numbers into L-bit drive words is as compact as possible.

3.4.1 Symbol Coding for N=3 (3-wire) differential signaling

For N=3, we encode 3 binary bits, whose valid values range from 0 to 5 (decimal), into a 3-bit drive word for the three differential transmitters (see Figure 3.1). The valid drive word codes are listed in Table 3.4.

Table 3.4 : Valid codes for 3-bit drive word on 3-wire signaling systems.

X_{In}	Y_{In}	Z_{In}
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0

The simplest implementation of this function is achieved by passing the input of the encoder unchanged to the output codes, wherever this does not result in an invalid drive word. This works for codes b{2:0}=001 (1dec) through b{2:0}=101 (5dec); the binary input value 000 can be mapped into the symbol 110 with some simple logic, as shown below in Figure 3.5.

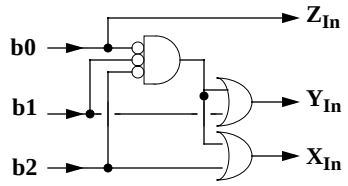


Figure 3.5. Simple binary to 3-wire-signaling encoding.

The corresponding decoder is shown in Figure 3.6.

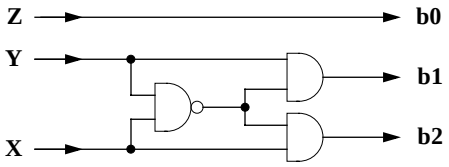


Figure 3.6. 3-wire to binary decoder.

A reversible truth table is shown below in Table 3.5.

Table 3.5 : Truth table for 3-wire encoding/decoding

b 2	b 1	b 0	X	Y	Z
0	0	0	1	1	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1

3.4.2 Symbol Coding for a 4-wire differential signaling system

For N=4, the symbol encoder must convert 5 binary bits (encoding decimal numbers 0 through 23) into 6 valid control bits X,Y,Z,U,V,W. This can be done with a lookup table, but simpler logic is possible. We next describe how one simplified encoder is obtained, again taking advantage of the fact that any permutation of the table also yields a valid encoding. First, we re-write the valid

codes on X..W, organized into 4 groups of 6 symbols that share like values on V,W. Reading these values from Table 3.2, we have the following list of valid drive word codes:

X	Y	Z	U	V	W
0	0	0	1	1	0
0	0	1	1	1	0
0	1	0	1	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	0	1
0	0	1	0	1	1
0	0	1	1	1	1
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	1	0	1	1
0	1	0	1	0	0
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	1	0	0	0	0
1	1	0	1	0	0

Note that the last row in the last group (V,W=00) is the inverse of the first row of the 3rd group (V,W=11); all of the elements of the second group are, in fact, inverses of some element of the first group. Next, the last row of the 2nd group (V,W=01) is the inverse of the first row of the 1rst group (V,W=10). Using these two observations, it is possible to construct an encoder using two 3-input, 4-output lookup tables of 6 entries each, a multiplexor, and a set of XOR functions.

We also note, however, that the codes for V,W=01 are a one-bit-left rotation of the codes for V,W=00 (Y–>X, Z–>Y, U–>Z, and X–>U, with a rearrangement of rows), so it is possible to use just one table, with 3 bits in and 6 valid combinations of 4 bits out. It can be any permutation of the table taken from the X,Y,Z,U sub-table with V,W=0,0:

0	1	0	1
1	0	0	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	0	1

Permuting the rows of this table so that the LSB alternates between 0 and 1, we have

0	1	0	1
1	0	0	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	0	0

An encoder based on this table was implemented in the Verilog hardware description language and synthesized using a simple CMOS standard cell library. It required only 18 gates from the library, and is shown in schematic form in Figure 3.7. The complexity of the corresponding decoder would be similar.

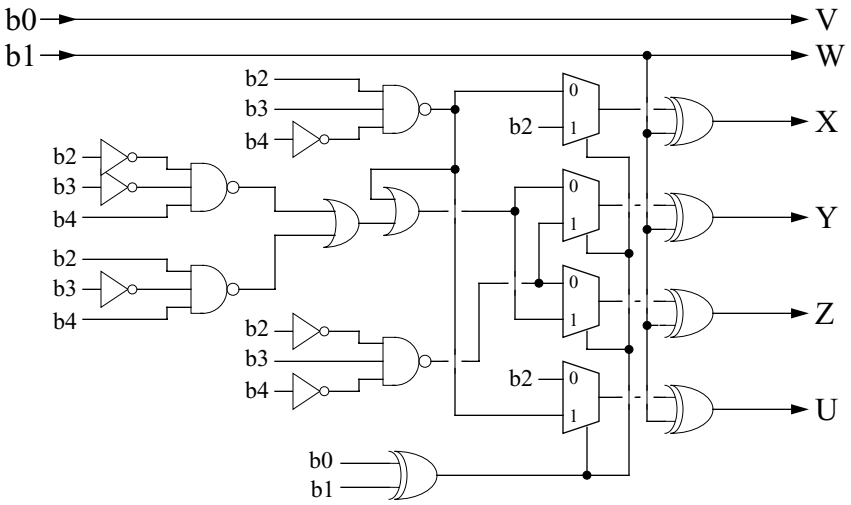


Figure 3.7. Schematic of a 4-wire symbol encoder.

3.4.3 Data Coding for a 4-wire differential signaling system.

So far, we have converted 5-bit symbol numbers into the valid 6-bit transmitter-drive codes for the 4-wire signaling system. Next we consider the problem of encoding binary data words of a more convenient size on a 4-wire channel.

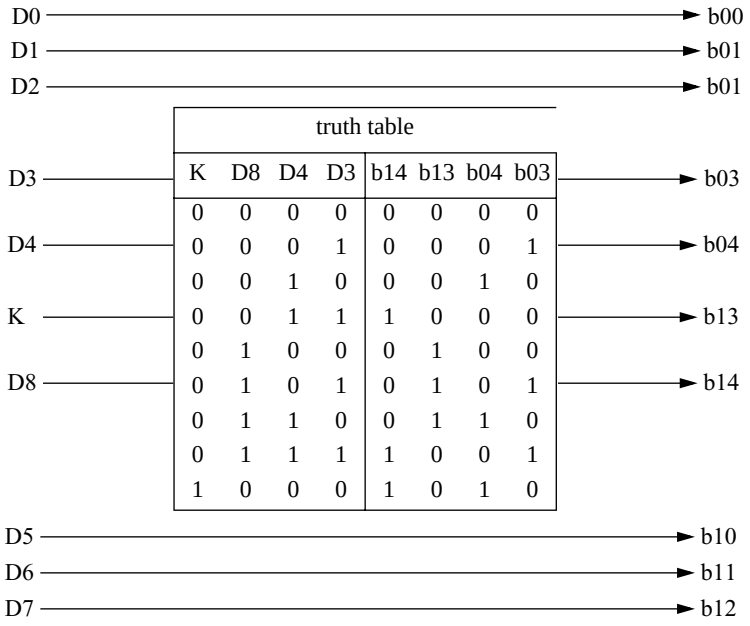
The first case considered is sending 9-bit data and some additional control words as two symbols on a 4-wire channel. This process encodes a 9-bit data word, D{8:0} into two 5-bit symbol numbers, b0{4:0} and b1{4:0}. Two instances of the logic described in Section 3.4.2 above are then used to drive the actual 4-wire line.

While any encoding of this sort can in principle be accomplished with a lookup table and implemented as a ROM, this particular table is large, and the tables for N greater than 4 would be prohibitive. So we look for ways to simplify the logic.

Since 8 is the largest power of 2 that is a common factor of 32 and 24, we pass the three ($\log_2$ 8) low-order bits right on through, and only have to process the remaining two bits. This idea is used twice in the actual encoder.

We encode 9 bits into 2 differential-quad symbols by passing 6 of those bits directly into the low-order bits of each symbol number, so that b00=D0, b01=D1, b02=D2, b10=D5, b11=D6, and b12=D7. Only the remaining 3 bits are passed through some logic to generate the high two bits of each diff-quad symbol.

These 4 functions of 3 bits turn out to be reasonably compact. Adding a 10th input bit, called "K" allows the transmission of 64 control words or "K characters" in addition to the 512 data values represented by the 9 input bits. This allows us to make use of all 567 unique states that can be represented by two differential-quad symbols. The complete encoder and decoder is expressed in the pseudo-schematic and truth table below in Figure 3.8.



truth table

K	D8	D4	D3	b14	b13	b04	b03
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	1	0

Figure 3.8. Psuedo-schematic for 9-bit data encoder.

Note that this psuedo schematic is the same for the decoder, but with inputs and outputs and the two planes of the table reversed. Schematics implementing both the encoder and decoder versions of the truth table are shown in Figure 3.9.

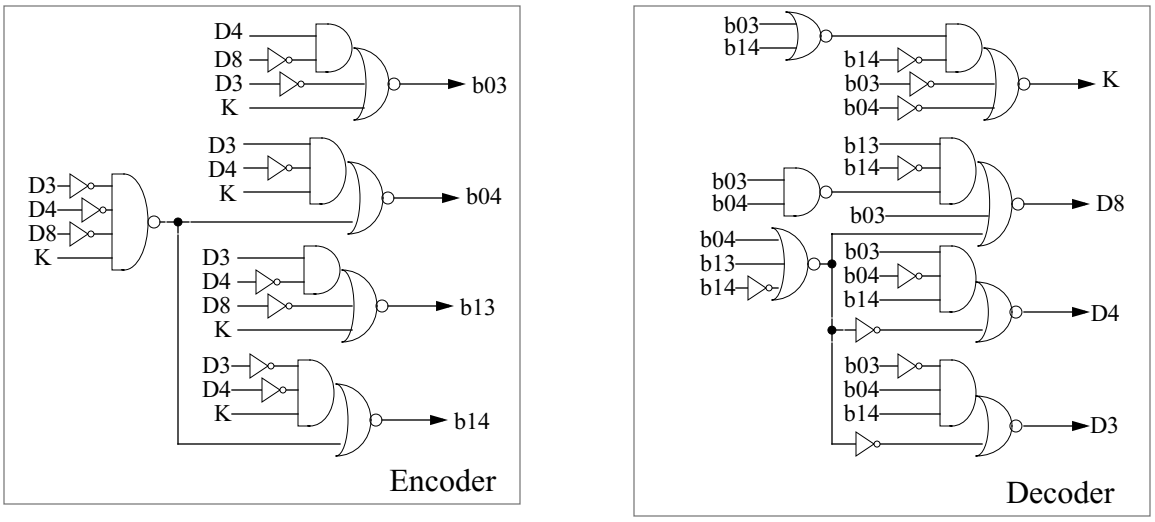


Figure 3.9. Logic schematics for encoder/decoder table.

4. Alternate forms of coding

4.1 DC Balanced Coding

The encoding schemes discussed so far have been designed to make the most efficient use of the available symbols for transfering data across the multiwire communications channel. Other considerations may require reserving some part of the symbol space to satisfy additional constraints. Chief among these constraints is the requirement in some situations for the currents in each wire from transmitter to reciever to have no DC component. One such situation is communicating across cables between cabinets that have seperate power supplies, in which it is desired to insert coupling capacitors in each communication wire to prevent DC currents from flowing from one power supply domain to another.

We have investigated this issue and at this point have a solution that requires 3 successive symbols to transmit 9 bits of information, DC-balanced. 50% overhead seems too large for this method to be practical. I may be feasible to ensure DC balance with better efficiency, and we will continue to investigate this issue.

5. Best Reduction to Practice

5.1 Voltage-mode vs Current-mode

Symbols transmitted on a wire can be represented either as current or voltage levels on the wire. Since current is converted to voltage in the terminator, this difference may appear to be trivial; however, the difference between the two modes of signaling is important in distinguishing implementations of data transmitters.

Multi-wire signaling is most easily expressed in a current-mode implementation. Signals from (N-1) of the N!/(2•(N-2)!) transmitters are summed onto each of the N wires in a multiwire system. Current summation is trivially accomplished by simply connecting the transmitter terminals to the wires. Voltage summation would require some way to add the voltages from multiple transmitters, before applying the summed voltage to the wire.

Although it appears that current-mode implementations of multi-wire signaling are preferred, a resistor network can be used as a simple means of connecting voltage-mode transmitters to a multi-wire transmission line, as shown in Figure 5.1; a 3-wire signaling system is used by way of example, but the generalization to N>3 is obvious. The external series resistors R_S convert the voltage outputs of the transmitters to currents, which are summed onto the three transmission line wires. Realizable voltage transmitters have non-zero internal impedance R_{int}. For proper impedance matching, $2 \bullet R_S + R_{int} = R_T$, where R_T is the termination resistance.

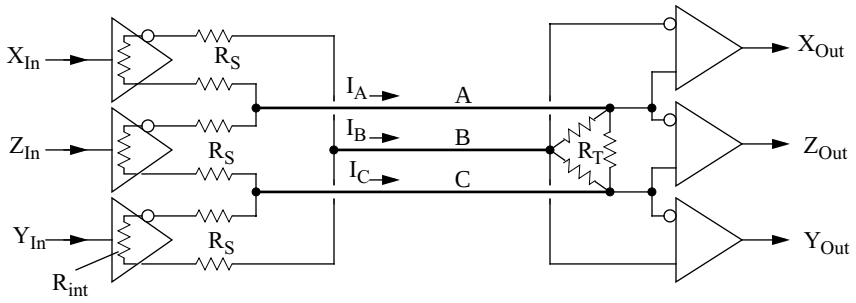


Figure 5.1. Resistor network for voltage-mode transmitters.

5.2 CMOS Current-mode Implementation

Current-mode transmitters can readily be implemented in CMOS technology. One possible implementation of a suitable current-mode transmitter is shown in Figure 5.2.

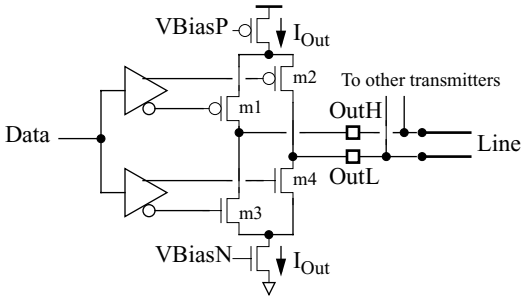


Figure 5.2. CMOS current-mode transmitters.

In this example, the "tail" transistors are biased into the linear or saturation region by setting VBiasN and VBiasP appropriately, so that both transistors are effectively current sources, and both carry the signaling current I_{Out}. The remaining four devices in the transmitter are arranged in

an “H-bridge” configuration and steer the output current into the Line, controlled by Data. When Data is HI, m1 and m4 are turned ON (m2, m3 OFF), so that I_{Out} is driven into OutH and pulled out of OutL; when Data is LO, m2,m3 are ON and the currents at the two output terminals are reversed.

Other configurations are possible, but all share the features of switching a current into the two halves of a differential transmission line. Note that ANSI LVDS (Low Voltage Differential Signaling) standard circuits could readily be used in a multi-wire signaling system with little or no changes (reference [10]).

5.3 Equalization

As explained in references [2,3], frequency dependent attentuation on realizable transmission lines leads to intersymbol interference. For fairly modest amounts of attenuation (6dB at the highest bit transmission frequency), this effect causes signals to become undetectable. Equalization can be used to extend the bit transmission frequency considerably. Equalization essentially introduces a filter, which can be placed into the transmission line at either the transmitter or receiver, that compensates for the frequency-dependent attenuation of the line. As explained in the references, it is easy to build an equalizing filter into the transmitter in a CMOS serial data link. This idea can be used effectively in multi-wire signaling, implemented essentially exactly as in the references. Each of the N!/(2•(N-2)!) “channels” on an N-wire transmission system can be equalized independently, since the waves on the line for each channel are independent, by the principal of superposition.

6. Review of Prior Art in Serial Communication Systems

The slightly related subject of ghost/wraith/phantom circuits (circuits that send data by differentially driving the common-mode signals on pairs of pairs) is described in reference [1].

CMOS serial links of various types are described in references [4,5,6,7,8,9, and 12].

Transmitter equalization, first described in [2], has been practiced more recently by others in [11 and 13]. An example of receiver equalization is described in [9].

The art of CMOS serial signaling links is reviewed in [14] and Chapter 11 of [15].

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