

Lab 5 – VGA Timing Generator

Due 2/17, 2:00 PM

Design a module (or modules) that generate VGA timing signals. For now you can test by making a higher-level module to display something interesting, like contrasting vertical lines, colored blocks, etc. Later you'll use this to build a character display.

Please see the lecture notes from Tuesday 2/10 for details.

I suggest that you proceed as follows.

1. First build a horizontal counter with a shorter count than you'd use for VGA, and test it on the simulator. Note that the only input is a clock, which you may want to count down to 25 MHz.
2. Add a hsync signal, again shorter than normal so you can simulate it in a short amount of time.
3. Use the horizontal counter to build a vertical (scan line) counter and test that design.
4. Finally, set your parameters for an actual VGA scan and try it on a CRT.

If you have any problems, use the logic analyzer to see what you are sending to the display. Even if you have no trouble with the design, I encourage you to try the logic analyzer.

Report

Demo the VGA generator to the LA.

Send a report by the deadline. It should include your project as a Zip file, and a short description of how you arrived at the design and your simulation/test strategy. Please include a copy of the Verilog code in the document so I can read it easily without running your ISE project.