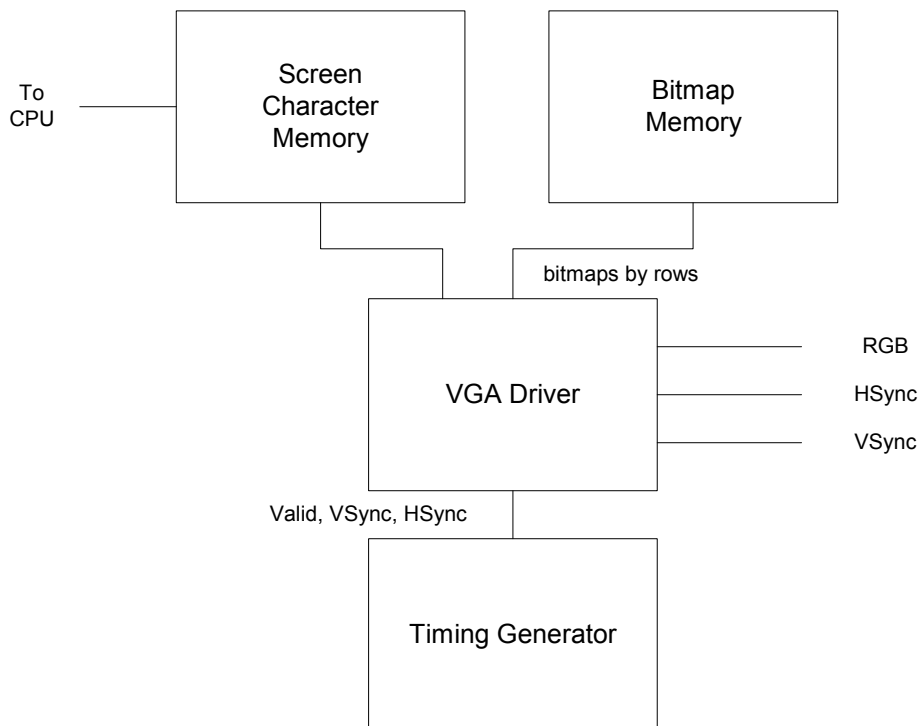


Finish the VGA Display

You have two lab periods to complete the VGA display.

Display

You'll need to add a character generator to your display-timing module from last time. I suggest an architecture like the following. The screen-character memory is dual ported. One port will eventually be mapped to CPU addresses so your program can write to the memory. For this lab just load something into the character memory.



The bitmap memory holds the dot matrix patterns of the characters. You should initialize this in the Verilog. A good source for character bitmaps is

<http://www.piclist.com/techref/datafile/charsets.htm>

You'll want to write a simple program to convert the bitmaps to the HEX codes that you need to initialize block RAM. A simple 5 by 7 character set expressed as a C struct is

<http://www.piclist.com/techref/datafile/charset/8x8.htm>

We talked about this in class.

The module that I've called *VGA driver* uses the Valid signal to gate red, green, and blue lines to drive the CRT. Since memory is limited, you may want to display characters in an area smaller than 640x480.

Suggested Strategy

This is starting to be a fairly complex design, and merits a careful test of submodules. Otherwise you'll have bugs but won't be able to figure out the problems.

Watch out to make sure you meet your timing constraints.

You can use some of the following techniques.

- Test memory accesses using a counter to run through memory. This is similar to the way my ramtest project works, except you can skip the 7-segment display.
- Perhaps test the use of the two memories, again by sending the result to output pins.
- Reduce the “size” of your screen and run in simulation. You should look to see whether you get the colors you expect at the right times. It's easy to be off by a clock because the memory accesses have to be pipelined.
- You can also run with reduced screen dimensions (it won't display on the monitor, of course) and look at the video on a logic analyzer. Remember that you can use the triggering features of the logic analyzers to start viewing wherever you want.

Conclusion

Show your working system to the LA.

Please send a description of your design, test strategy (important) and a zip file of the project.