MONTEK SINGH – CURRICULUM VITAE

Associate Professor
Dept. of Computer Science
Univ. of North Carolina at Chapel Hill
Sitterson Hall, Campus Box 3175
Chapel Hill, NC 27599, USA
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EDUCATION

Columbia University, New York, NY	Computer Science	Ph.D., February 2002
Columbia University, New York, NY	Computer Science	M.S., October 1996
Indian Institute of Technology, Delhi, India	Electrical Engineering	B.Tech, May 1993

PROFESSIONAL EXPERIENCE

7/1/07-present	Associate Professor (tenured), Dept. of Computer Science, UNC Chapel Hill
8/15/23-present	Associate Chair for Academic Affairs, Dept. of Computer Science, UNC Chapel Hill
8/1/01-6/30/07	Assistant Professor, Dept. of Computer Science, UNC Chapel Hill
8/21/94-12/31/01	Graduate Research Assistant, Dept. of Computer Science, Columbia University, NY
7/31/00-12/31/00	Summer Intern, IBM T.J. Watson Research Center, Yorktown Heights, NY
6/2/97-8/29/97	Summer Intern, Intel Corp., Santa Clara, CA
6/1/99-8/31/99	Academic Visitor, Amulet Group, University of Manchester, Manchester, UK
1992 Summer	Practical Trainee, Bhabha Atomic Research Center, Bombay, India

HONORS

- **Tanner Award for Excellence in Undergraduate Teaching,** a campus-level teaching award, Feb 2026.
- **Graduate Teaching Award,** Dept. of Computer Science, awarded by the graduate student association (CSSA), May 2021.
- **Graduate Teaching Award,** Dept. of Computer Science, awarded by the graduate student association (CSSA), May 2019.
- **Integrated Curriculum Award** for development of new First-Year Seminar ($10K for course development) for "Lux Libertas: On the Knowledge, Handling and Display of Light." October 2019.
- **Excellence in Undergraduate Teaching Award,** Dept. of Computer Science, awarded by the Computer Science Club (undergraduate computer science students organization), May 2017.
- **Excellence in Undergraduate Teaching Award,** Dept. of Computer Science, awarded by the Computer Science Club (undergraduate computer science students organization), May 2014.
- **Best Paper Award,** IEEE VR 2016 Conference, Greenville, South Carolina, March 2016. (International Annual Symposium on Virtual Reality)

- **Best Paper Finalist,** 14th IEEE ASYNC Symposium, Newcastle, UK, April 2008. (International Symposium on Asynchronous Circuits and Systems)

- **Best Paper Finalist,** 8th IEEE ASYNC Symposium, Manchester, UK, April 2002. (International Symposium on Asynchronous Circuits and Systems)

- **Best Paper Award,** 6th IEEE ASYNC Symposium, Eilat, Israel, April 2000. (International Symposium on Asynchronous Circuits and Systems)

- IBM Faculty Award, August 2004.

- DARPA CLASS Grant Award, March 2005.

- UNC Junior Faculty Development Award, November 2002.

BIBLIOGRAPHY and PRODUCTS

Patents:

- (Issued) Camera sensor with event token based image capture and reconstruction. U.S. Letters Patent No. 10,250,824 issued April 2, 2019.

- (Issued) Systems, pipeline stages, and computer readable media for advanced asynchronous pipeline circuits. U.S. Letters Patent No. 8,872,544 issued October 28, 2014.

- (Issued) Systems, pipeline stages, and computer readable media for advanced asynchronous pipeline circuits. U.S. Letters Patent No. 8,669,779 issued March 11, 2014.

- (Issued) Circuits and methods for high-capacity asynchronous pipeline processing, US Patent 7,053,665 granted May 30, 2006.

- (Issued) Asynchronous pipeline with latch controllers, US Patent 6,958,627 granted October 25, 2005.

- (Issued) Circuits and methods for high-capacity asynchronous pipeline, US Patent 6,867,620 granted March 15, 2005.

- (Issued) High-throughput asynchronous dynamic pipelines, US Patent 6,590,424 granted July 8, 2003.

Dissertations

- M. Singh. *The Design of High-Throughput Asynchronous Pipelines.* Ph.D. Thesis, Columbia University, New York, NY, December 2001.

- A. Chatterjee and M. Singh. *Genetic Algorithms for the Subgraph Isomorphism Problem.* B.Tech. Thesis, Indian Institute of Technology, New Delhi, India, May 1993.

Journals Edited

- Luciano Lavagno and Montek Singh (Eds.). Asynchronous Design [Special Issue]. *IEEE Design & Test of Computers (D&T),* vol. 28, no. 5, September/October 2011.
- Montek Singh and Steven M. Nowick (Eds.). Asynchrony in System Design [Special Issue]. *ACM Journal on Emerging Technologies in Computing Systems (JETC),* vol. 7, no. 4, December 2011.

Book Chapters

- Montek Singh. "Asynchronous Sensing." Chapter 6 in Asynchronous Circuit Applications [Eds. Jia Di and Scott C. Smith]. Publisher: The Institution of Engineering and Technology. Pages 97-112, November 2019. Book DOI: 10.1049/PBCS061E. e-ISBN: 9781785618185.

JOURNAL ARTICLES (published, refereed)

- A. Blate, M. Whitton, M. Singh, G. Welch, A. State, T. Whitted, H. Fuchs. "Implementation and Evaluation of a 50 kHz, 28us Motion-to-Pose Latency Head Tracking Instrument." *IEEE Transactions on Visualization and Computer Graphics*, vol. 25, no. 5, pages 1970-1980, May 2019.

- P. Lincoln, A. Blate, M. Singh, T. Whitted, A. State, A. Lastra, and H. Fuchs. "From Motion to Photons in 80 Microseconds: Towards Minimal Latency for Virtual and Augmented Reality." *IEEE Transactions on Visualization and Computer Graphics (TVCG)*, vol. 22, no. 4, pages 1367-1376, April 2016. (**Best Paper Award** at IEEE VR 2016)

- S.M. Nowick and M. Singh. "Asynchronous Design -- Part 1: Overview and Recent Advances." *IEEE Design and Test (D&T),* vol. 32, no. 3, pages 5-18, June 2015.

- S.M. Nowick and M. Singh. "Asynchronous Design -- Part 2: Systems and Methodologies." *IEEE Design and Test (D&T),* vol. 32, no. 3, pages 19-28, June 2015.

- S.M. Nowick and M. Singh. "High-Performance Asynchronous Pipelines: An Overview." *IEEE Design and Test of Computers (D&T),* special issue on Asynchronous Design, vol. 28, no. 5, pages 8-22, September/October 2011.

- J. Pool, A. Lastra and M. Singh. "Power-Gated Arithmetic Circuits for Energy-Precision Tradeoffs in Mobile Graphics Processing Units." *Journal of Low-Power Electronics (JOLPE),* vol. 7, no. 2, pages 148-162, April 2011. American Scientific Publishers, doi:10.1166/jolpe.2011.1124.

- M. Singh, J.A. Tierno, A. Rylyakov, S. Rylov, and S.M. Nowick. "An Adaptively-Pipelined Mixed Synchronous-Asynchronous Digital FIR Filter Chip Operating at 1.3 Gigahertz." *IEEE Transactions on VLSI Systems (TVLSI),* vol. 18, no. 7, pages 1043-1056, July 2010.

- M. Singh and S.M. Nowick. "The Design of High-Performance Dynamic Asynchronous Pipelines: Lookahead Style." *IEEE Transactions on VLSI Systems (TVLSI),* vol. 15, no. 11, pages 1256-1269, November 2007.

- M. Singh and S.M. Nowick. "The Design of High-Performance Dynamic Asynchronous Pipelines: High-Capacity Style." *IEEE Transactions on VLSI Systems (TVLSI),* vol. 15, no. 11, pages 1270-1283, November 2007.

- M. Singh and S.M. Nowick. "MOUSETRAP: High-Speed Transition-Signaling Asynchronous Pipelines." *IEEE Transactions on VLSI Systems (TVLSI),* vol. 15, no. 6, pages 684-698, June 2007.

- M. Singh and S.M. Nowick. "Synthesis for Logical Initializability of Synchronous Finite State Machines." *IEEE Transactions on VLSI Systems (TVLSI),* vol. 8, no. 5, pages 542-557, October 2000.

- M. Singh, A. Chatterjee, and S. Chaudhury. "Matching Structural Shape Descriptions Using Genetic Algorithms." *Pattern Recognition,* vol. 30, no. 9, pages 1451-1462, September 1997 (Elsevier Science, UK).

CONFERENCE PAPERS (published, refereed)

- A.C. Freeman, K. Mayer-Patel, and M. Singh. "Accelerated Event-Based Feature Detection and Compression for Surveillance Video Systems." In *Proceedings of the 15th ACM Multimedia Systems Conference* (MMSys 2024), April 2024, Bari, Italy, pages 132-143.

- A.C. Freeman, M. Singh, and K. Mayer-Patel. "An Asynchronous Intensity Representation for Framed and Event Video Sources." *Proc. of the 14th ACM Multimedia Systems Conference* (MMSys 2023), June 2023, Vancouver, BC, Canada. ACM, New York, NY, USA, pages 74-85. DOI: https://doi.org/10.1145/3587819.3590969

- A. Smith, M. Singh, and K. Mayer-Patel. "A System Model For Frameless Asynchronous High Dynamic Range Sensors." *Proc. ACM SIGMM Workshop on Network and Operating Systems Support for Digital Audio and Video* (MMSYS/NOSSDAV-17), pages 85-90, Taipei, Taiwan, June 2017. DOI: https://doi.org/10.1145/3083165.3083178

- M. Singh, P. Zhang, A. Vitkus, K. Mayer-Patel, and L. Vicci. "A Frameless Imaging Sensor with Asynchronous Pixels: An Architectural Evaluation." *Proc. Intl. Symp. on Asynchronous Circuits and Systems* (ASYNC-17), pages 110-117, San Diego, May 2017.

- P. Lincoln, A. Blate, M. Singh, A. State, T. Whitted, M. Whitton, A. Lastra, and H. Fuchs. "Scene-Adaptive High Dynamic Range Display for Low Latency Augmented Reality." *Proc. of the ACM SIGGRAPH Symposium on Interactive 3D Graphics and Games (i3D-17),* pages 1-7, San Francisco, CA, February 2017.

- V. Gupta and M. Singh. "Energy Conservation in Asynchronous Systems using Self-Adaptive Fine-Grain Voltage Scaling." *Proc. of the 4th IEEE Intl. Green Computing Conference (IGCC-13),* pages 1-8, Arlington, VA, June 2013.

- J. Hansen and M. Singh. "A Fast Hierarchical Approach to Resource Sharing in Pipelined Asynchronous Systems." *Proc. of the 18th IEEE Intl. Symposium on Asynchronous Circuits and Systems (ASYNC-12),* pages 57-64, Lyngby, Denmark, May 2012.

- J. Hansen and M. Singh. "Multi-Token Resource Sharing for Pipelined Asynchronous Systems." *Proc. of ACM/IEEE Design, Automation and Test in Europe (DATE-2012),* pages 1191-1196, Dresden, Germany, March 2012.

- J. Pool, A. Lastra and M. Singh. "Lossless Compression of Variable-Precision Floating-Point Buffers on GPUs." *Proc. of the ACM SIGGRAPH Symposium on Interactive 3D Graphics and Games (I3D-2012),* pages 47-54, Costa Mesa, CA, March 2012.

- J. Pool, A. Lastra and M. Singh. "Precision Selection for Energy-Efficient Pixel Shaders." *Proc. of High-Performance Graphics (HPG-2011),* pages 159-168,Vancouver, Canada, August 2011.

- J. Hansen and M. Singh. "An Energy and Power-Aware Approach to High-Level Synthesis of Asynchronous Systems." *Proc. of IEEE/ACM Intl. Conf. on Computer-Aided Design (ICCAD-10),* pages 269-276, San Jose, CA, November 2010.

- J. Pool, A. Lastra, and M. Singh. "An Energy Model for Graphics Processing Units." *Proc. of IEEE Intl. Conf. on Computer Design (ICCD-10),* pages 409-416, Amsterdam, the Netherlands, October 2010.

- J. Hansen and M. Singh. "A Fast Branch-and-Bound Approach to High-Level Synthesis of Asynchronous Systems." *Proc. of the 16th IEEE Intl. Symp. on Async. Circ. and Syst. (ASYNC-10),* pages 107-116, Grenoble, France, May 2010.

- G. Gill and M. Singh. "Automated Microarchitectural Exploration for Achieving Throughput Targets in Pipelined Asynchronous Systems." *Proc. of the 16th IEEE Intl. Symp. on Async. Circ. and Syst. (ASYNC-10),* pages 117-127, Grenoble, France, May 2010.

- G. Gill and M. Singh. "Bottleneck Analysis and Alleviation in Pipelined Systems: A Fast Hierarchical Approach." *Proc. of the 15th IEEE Intl. Symp. on Async. Circ. and Syst. (ASYNC-09),* pages 195-205, Chapel Hill, NC, May 2009.

- G. Gill, J. Hansen, A. Agiwal, L. Vicci and M Singh. "A High-Speed GCD Chip: A Case Study in Asynchronous Design." *Proc. of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI-09),* pages 205-210, Tampa, FL, May 2009.

- G. Gill, V. Gupta, and M. Singh. "Performance Estimation and Slack Matching for Pipelined Asynchronous Architectures with Choice." *Proc. of IEEE/ACM Intl. Conf. on Computer-Aided Design (ICCAD-08)*, pages 449-456, San Jose, CA, November 2008.

- J. Pool, A. Lastra, and M. Singh. "Energy-Precision Tradeoffs in Mobile Graphics Processing Units." *Proc. of IEEE Intl. Conf. on Computer Design (ICCD-08),* pages 60-67, Lake Tahoe, CA, October 2008.

- J. Hansen and M. Singh. "Concurrency-Enhancing Transformations for Asynchronous Behavioral Specifications: A Data-Driven Approach." *Proc. of the 14th IEEE Intl. Symp. on Async. Circ. and Syst. (ASYNC-08),* pages 15-25, Newcastle, UK, April 2008. **(Best Paper Finalist)**

- G. Gill, J. Hansen and M. Singh. "Loop Pipelining for High-Throughput Stream Computation Using Self-Timed Rings." *Proc. of Intl. Conf. on Computer-Aided Design (ICCAD-06),* pages 289–296, San Jose, CA, November 2006.

- M. Ampalam and M. Singh. "Counterflow Pipelining: Architectural Support for Preemption in Asynchronous Systems using Anti-Tokens." *Proc. of Intl. Conf. on Computer-Aided Design (ICCAD-06),* pages 611–618, San Jose, CA, November 2006.

- G. Gill, A. Agiwal, M. Singh, F. Shi, and Y. Makris. "Low-Overhead Testing of Delay Faults in High-Speed Asynchronous Pipelines." *Proc. of the 12th IEEE Intl. Symp. on Async. Circ. and Syst. (ASYNC-06),* pages 46-56, Grenoble, France, March 2006.

- A. Agiwal and M. Singh. "An Architecture and Wrapper Synthesis for Multi-Clock Latency-Insensitive Systems." *Proc. of Intl. Conf. on Computer-Aided Design (ICCAD-05),* pages 1006–1013, San Jose, CA, November 2005.

- F. Shi, Y. Makris, S.M. Nowick and M. Singh. "Test Generation for Ultra-High-Speed Asynchronous Pipelines." *Proc. of Intl. Test Conference (ITC-05),* pages 1009-1018, Austin, TX, November 2005.

- J. Hensley, T. Scheuermann, G. Coombe, A. Lastra and M. Singh. "Fast Summed-Area Table Generation and its Applications." *Proc. of Eurographics 2005,* pages 547–555, Dublin, Ireland, August 2005.

- J. Hensley, M. Singh, A. Lastra. "A Fast, Energy-Efficient Z-Comparator." *Proc. of the ACM SIGGRAPH/EUROGRAPHICS Conference on Graphics Hardware (GHW-05),* pages 41–44, Los Angeles, CA, July 2005.

- A. Agiwal and M. Singh. "Multi-Clock Latency-Insensitive Architecture and Wrapper Synthesis." *Proc. of the Second Intl. Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Design (FMGALS-05),* in cooperation with ACM SIGDA and SIGARCH, Verona, Italy, July 2005. Published in Electronic Notes in Theoretical Computer Science, vol. 146, no. 2, pages 5-28, January 2006. (ISSN: 1571-0661, Elsevier) https://doi.org/10.1016/j.entcs.2005.05.033

- J. Hensley, A. Lastra and M. Singh. "A Scalable Counterflow-Pipelined Asynchronous Radix-Four Booth Multiplier." *Proc. of the 11th IEEE Intl. Symp. on Async. Circ. and Syst. (ASYNC-05),* pages 128–137, New York City, NY, March 2005.

- J. Hensley, A. Lastra and M. Singh. "An Area- and Energy-Efficient Asynchronous Booth Multiplier for Mobile Devices." *Proc. of IEEE Intl. Conf. on Computer Design (ICCD-04),* pages 18–25, San Jose, CA, October 2004.

- M. Singh and M. Theobald. "Generalized Latency-Insensitive Systems for Single-Clock and Multi-Clock Architectures." *Proc. of ACM/IEEE Design, Automation and Test in Europe (DATE-04),* pages 1008–1013, Paris, France, February 2004.

- M. Singh, J.A. Tierno, A. Rylyakov, S. Rylov, and S.M. Nowick. "An Adaptively-Pipelined Mixed Synchronous-Asynchronous Digital FIR Filter Chip Operating at 1.3 Gigahertz." *Proc. of the 8th IEEE Intl. Symp. on Async. Circ. and Syst. (ASYNC-02),* pages 84–95, Manchester, UK, April 2002. **(Best Paper Finalist)**

- R.O. Ozdag, M. Singh, P.A. Beerel, and S.M. Nowick. "High-Speed Non-Linear Asynchronous Pipelines." *Proc. of Design, Automation and Test in Europe (DATE-02),* pages 1000–1007, Paris, France, March 2002.

- J. Tierno, A. Rylyakov, S. Rylov, M. Singh, P. Ampadu, S.M. Nowick, M. Immediato, and S. Gowda. "A 1.3 GSample/s 10-tap Full-rate Variable-latency Self-timed FIR filter with Clocked Interfaces." *Proc. of IEEE Intl. Solid-State Circ. Conf. (ISSCC-02),* 7 pages (3 pages in vol. 1, 4 pages in vol. 2), San Francisco, CA, February 2002.

- M. Singh and S.M. Nowick. "MOUSETRAP: Ultra-High-Speed Transition-Signaling Asynchronous Pipelines." *Proc. of IEEE Intl. Conf. on Computer Design (ICCD-01),* pages 9–17, Austin, TX, September 2001.

- M. Singh and S.M. Nowick. "High-Throughput Asynchronous Pipelines for Fine-Grain Dynamic Datapaths." *Proc. of the 6th IEEE Intl. Symp. on Adv. Res. in Async. Circ. and Syst. (ASYNC-2000),* pages 198–209, Eilat, Israel, April 2000. **(Received Best Paper Award)**

- M. Singh and S.M. Nowick. "Fine-Grain Pipelined Asynchronous Adders for High-Speed DSP Applications." *Proc. of IEEE Computer Society Annual Workshop on VLSI (WVLSI-2000),* pages 111-118, Orlando, FL, April 2000. (IEEE Computer Society Press, ISBN: 0-7695-0534-1)

- M. Singh and S.M. Nowick. "Synthesis for Logical Initializability of Synchronous Finite State Machines." *Proc. of the Tenth Intl. Conf. on VLSI Design (VLSID-97),* pages 76–80, Hyderabad, India, January 1997.

- M. Singh and S.M. Nowick. "Synthesis for Initializability of Asynchronous Sequential Machines." *Proc. of the Intl. Test Conference (ITC-96),* pages 232–241, Washington, DC, October 1996.

WORKSHOP PAPERS (refereed, limited distribution in workshop proceedings)

- Yi Hu, Abu-Bakar Raja, Ketan Mayer-Patel and Montek Singh. "Asynchronous Pixels for Astronomical Imaging." *Proc. of the Fresh Ideas Workshop, IEEE Intl. Symposium on Asynchronous Circuits and Systems (ASYNC 2019),* Hirosaki, Japan, May 2019.

- C. Arnott, L. Vicci, and M. Singh. "IMAGIN: A Frameless HDR Camera Sensor." *Proc. of the Fresh Ideas Workshop, IEEE Intl. Symposium on Asynchronous Circuits and Systems (ASYNC 2015),* Mountain View, CA, May 2015.

- G. Gill and M. Singh. "A Heuristic Approach to Bottleneck Removal in Asynchronous Pipelined Systems." *Proc. of the 18th IEEE/ACM Intl. Workshop on Logic and Synthesis (IWLS-09),* Berkeley, CA, July 2009.

- G. Gill, V. Gupta, and M. Singh. "Performance Estimation and Slack Matching for Pipelined Asynchronous Architectures with Choice." *Proc. of the 17th IEEE/ACM Intl. Workshop on Logic and Synthesis (IWLS-08),* Lake Tahoe, CA, June 2008.

- G. Gill and M. Singh. "Robust Synthesis of Asynchronous Burst-Mode Machines." *Proc. of the 14th IEEE/ACM Intl. Workshop on Logic and Synthesis (IWLS-05),* Lake Arrowhead, CA, June 2005.

- G. Gill and M. Singh. "Synthesizing Asynchronous Burst-Mode Machines without the Fundamental-Mode Timing Assumption." *Proc. of the ACM/IEEE Intl. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU-05),* San Francisco, CA, February 2005.

- M. Singh and M. Theobald. "Generalized Latency-Insensitive Systems for GALS Architectures." *Proc. of the Workshop on Formal Methods for Globally Asynchronous Locally Synchronous (GALS) Architecture (FMGALS-03),* held in conjunction with the 12th International Formal Methods Europe Symposium, Pisa, Italy, September 2003.

- M. Singh and S.M. Nowick. "MOUSETRAP: Ultra-High-Speed Transition-Signaling Asynchronous Pipelines." *Proc. of the ACM/IEEE Intl. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU-2000),* Austin, TX, December 2000.

- Stephen B. Furber, A. Efthymiou and M. Singh. "A Power-Efficient Duplex Communication System." *Workshop on Asynchronous Interfaces: Tools, Techniques and Implementations,* TU Delft, the Netherlands, July 2000.

- Montek Singh and Steven M. Nowick. "State Assignment for Initializability of Synchronous Finite State Machines." *IEEE Intl. Test Synthesis Workshop (ITSW-06),* Santa Barbara, CA, May 1996.

POSTERS, SKETCHES and ABSTRACTS (refereed)

- Yi Hu, Abu-Bakar Raja, Ketan Mayer-Patel and Montek Singh. "Asynchronous Pixels for Astronomical Imaging." Poster presented at *IEEE Intl. Symposium on Asynchronous Circuits and Systems (ASYNC 2019),* Hirosaki, Japan, May 2019.

- J. Hensley, T. Scheuermann, M. Singh, and A. Lastra. "Fast Summed-Area Table Generation for Glossy Environmental Reflections," Sketch presented at SIGGRAPH 2005, Los Angeles, CA, August 2005.

- J. Hensley, T. Scheuermann, M. Singh, and A. Lastra. "Fast, Approximate HDR Image-Based Lighting Using Summed-Area Tables." Poster to be presented at Symposium on Interactive 3D Graphics and Games (i3D-07), Seattle, WA, April 2007.

- G. Gill and M. Singh. "Ray Tracing on Asynchrounous Supercomputing Stream Processors." Poster presented at the IEEE Symposium on Interactive Ray Tracing, Salt Lake City, Utah, September 2006.

- G. Gill, J. Hansen and M. Singh. "High-Throughput Looping in Stream Processors Using Self-Timed Architectures." Poster and abstract at the Workshop on Edge Computing Using New Commodity Architectures (EDGE), Chapel Hill, NC, May 2006.

- M. Singh, "The Design of High-Speed Asynchronous Pipelines." Poster presented at the ACM SIGDA Ph.D. Forum, held in conjunction with the Design Automation Conference (DAC-01), Las Vegas, NV, June 2001.

WORKSHOP PAPER (not refereed, limited distribution in workshop proceedings)

- Montek Singh and Steven M. Nowick, "Gate-Level Pipelines for High Throughput." *Proc. of the 6th UK Asynchronous Forum,* Manchester, UK, July 1999.

TEACHING ACTIVITIES

- *Digital Logic and Computer Design* (Comp541), Spring 2027: 50 students (expected).
- *Computational Photography* (Comp572), Fall 2026: 70 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2026: 31 students.
- *Computational Photography* (Comp572), Fall 2025: 72 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2025: 37 students.
- *Digital Logic and Computer Design* (Comp541), Fall 2024: 32 students.
- *Lux Libertas (Comp590-084 and RELI89),* an Integrated Curriculum first-year seminar (IC FYS) taught jointly with Prof. Todd Ochoa of the Dept. of Religious Studies, Spring 2024: 36 students.
- *Digital Logic and Computer Design* (Comp541), Fall 2023: 40 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2023: 45 students.
- *Computational Photography* (Comp572), Fall 2022: 105 students.
- *Digital Logic and Computer Design* (Comp541), Fall 2022: 40 students.
- *Computational Photography* (Comp572), Spring 2022: 105 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2022: 45 students.
- *Digital Logic and Computer Design* (Comp541), Fall 2021: 45 students.
- *Lux Libertas (Comp590-084 and RELI89),* an Integrated Curriculum first-year seminar (IC FYS) taught jointly with Prof. Todd Ochoa of the Dept. of Religious Studies, Fall 2021: 24 students.
- *Computational Photography* (Comp572), Spring 2021: 90 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2021: 45 students.
- *Computational Photography* (Comp572), Fall 2020: 32 students.
- *Digital Logic and Computer Design* (Comp541), Fall 2020: 40 students.
- *Computer Organization and Design* (Comp411), Spring 2020: 165 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2020: 45 students.
- *Computer Organization and Design* (Comp411), Fall 2019: 180 students.
- *Lux Libertas (Comp89-084 and RELI89),* an Integrated Curriculum first-year seminar (IC FYS) taught jointly with Prof. Todd Ochoa of the Dept. of Religious Studies, Fall 2019: 24 students.
- *Computational Photography* (Comp790-084), Spring 2019: 20 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2019: 34 students.
- *Computer Organization and Design* (Comp411), Fall 2018: 128 students.
- *Digital Logic and Computer Design* (Comp541), Fall 2018: 34 students.
- *Computer Organization and Design* (Comp411), Spring 2018: 125 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2018: 39 students.
- *Computer Organization and Design* (Comp411), Fall 2017: 120 students.
- *Digital Logic and Computer Design* (Comp541), Fall 2017: 35 students.
- *Computer Organization and Design* (Comp411), Spring 2017: 88 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2017: 39 students
- *Digital Logic and Computer Design* (Comp541), Fall 2016: 40 students.
- *Computer Architecture* (Comp740), Fall 2016: 14 students.

- *Computer Organization and Design* (Comp411), Spring 2016: 145 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2016: 38 students.
- *Computer Organization and Design* (Comp411), Fall 2015: 65 students.
- *Digital Logic and Computer Design* (Comp541), Fall 2015: 35 students.
- *Computer Architecture* (Comp740), Spring 2015: 10 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2015: 34 students.
- *Digital Logic and Computer Design* (Comp541), Fall 2014: 37 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2014: 49 students.
- *Computer Architecture* (Comp740), Spring 2014: 6 students.
- *Computer Organization and Design* (Comp411), Fall 2013: 95 students.
- *Computer Organization and Design* (Comp411), Fall 2012: 80 students.
- *Digital Logic and Computer Design* (Comp541), Spring 2012: 38 students.
- *Emerging Technologies of Computation* (Comp790), Fall 2011: 2 students (research seminar).
- *Computer Organization and Design* (Comp411), Spring 2011: 55 students.
- *Computer Organization and Design* (Comp411), Fall 2010: 25 students.
- *Digital Logic* (Comp541), Spring 2010: 10 students.
- *Computer Organization and Design* (Comp411), Fall 2009: 35 students.
- *Computer Architecture* (Comp206), Spring 2009: 12 students.
- *Computer Organization and Design* (Comp411), Fall 2008: 33 students.
- *Computer Organization and Design* (Comp411), Spring 2008: 40 students.
- *Introduction to Clockless Computing* (Comp790), Fall 2007: 5 students.
- *Digital Logic* (Comp541), Spring 2007: 6 students.
- *Clockless Computing and Silicon Compilers* (Comp290), Spring 2006: 7 students.
- *Computer Architecture* (Comp206), Fall 2005: 30 students.
- *Introduction to VLSI Design* (Comp268), Spring 2005: 4 students.
- *Computer Architecture* (Comp206), Fall 2004: 25 students.
- *Asynchronous Systems and Introduction to VLSI Design* (Comp290), Spring 2004: 7 students.
- *Computer Architecture* (Comp206), Fall 2003: 30 students.
- *Introduction to Asynchronous Design* (Comp290), Spring 2003: 4 students.
- *Computer Architecture* (Comp206), Fall 2002: 17 students.
- *Elements of Hardware Systems* (Comp261), co-taught with Lea Vicci, Spring 2002: 7 students.
- *High-Speed Asynchronous Pipelines* (Comp290), Fall 2001: 7 students and 3 faculty.

PH.D. STUDENTS SUPERVISED

- **Andrew C. Freeman** (Fall 2021-Summer 2024), joint with Prof. Ketan Mayer-Patel. Graduated with Ph.D. degree in Summer 2024; employed at Baylor University, TX. Ph.D. Thesis: *Rethinking Video with a Universal Event-Based Representation.*

- **Jeff Pool** (Fall 2007-Spring 2012), joint with Prof. Anselmo Lastra. Graduated with Ph.D. degree in Spring 2012; employed by Nvidia, Inc., Durham, NC. Ph.D. Thesis: *Energy-Precision Tradeoffs in the Graphics Pipeline.*

- **John Hansen** (Fall 2005-Spring 2012). Graduated with Ph.D. degree in Spring 2012. Ph.D. Thesis: *A Behavioral Design Flow for Synthesis and Optimization of Asynchronous Systems.*

- **Gennette Gill** (Fall 2003-Spring 2010). Graduated with Ph.D. degree in Spring 2010; employed by D.E. Shaw Research, New York. Ph.D. Thesis: *Analysis and Optimization of Pipelined Asynchronous Systems.*

- **Justin Hensley** (Fall 2003-Fall 2006), joint with Prof. Anselmo Lastra: Graduated with Ph.D. degree; employed by AMD/ATI. Ph.D. Thesis: *Improving the Rendering Quality of Graphics Hardware.*

M.S. STUDENTS SUPERVISED (for research)

- **Andrew Vitkus** (Fall 2019-Fall 2020): Graduated with M.S. degree. M.S. Thesis: *Optimizing Throughput and Energy via Fine-Grain Dynamic Voltage Scaling in Elastic Dataflow Systems.*
- **Abu-Bakar Raja** (Spring 2018-Fall 2018): Graduated with M.S. degree. M.S. Paper: *Design and Optimization of Pixel Circuitry for a Frameless Imaging System.*
- **Andrew Vitkus** (Fall 2017-Fall 2018): Research topic: Frameless high-dynamic-range image sensors.
- **Manoj Ampalam** (Fall 2005-Spring 2006): Graduated with M.S. degree; employed by Microsoft Research. M.S. Thesis: *Counterflow Pipelining for Preemption in Asynchronous Systems.*
- **Ankur Agiwal** (Fall 2004-Fall 2005): Graduated with M.S. degree; employed by Microsoft Research.
- **Vishal Gupta** (Fall 2006-Spring 2007): Graduated with M.S. degree. M.S. Thesis: *Dynamic voltage scaling for energy conservation.*
- **Pintian Zhang** (Fall 2015-Spring 2016): Graduate with M.S. degree. M.S. Thesis: *A Frameless Imaging System: Architectural Design and Simulation.*

UNDERGRADUATE STUDENTS SUPERVISED (for research)

- **Joaquim Joel D'Silva** (Summer 2026-present): Honor's Thesis: Physical design of an event camera sensor.
- **Finn Stewart James** (Fall 2021-Spring 2022): Research Topic: User-Interface Front-End for Video Triage.
- **Yi Hu** (Fall 2018-Spring 2019). Honor's Thesis: A frameless image sensor with application to astronomy.
- **Colin Arnott** (Spring 2015): Research topic: Frameless high-dynamic-range image sensors.
- **Andrew Vitkus** (Fall 2016-Spring 2017): Research topic: Frameless high-dynamic-range image sensors.

PH.D. COMMITTEES

- **Jaehyun Han** (2022-2024). Research Topic: Reduced Associativity Memory Mapping in Computer Systems.
- **Yubo Luo** (2022-2023). Research Topic: Efficient Task Execution on Resource-Constrained Systems.
- **Sims Osborne** (2022-2023). Research Topic: Using Simultaneous Multithreading to Support Real-Time Scheduling.
- **Andrew Freeman** (2020-2024). Research Topic: Representation and Streaming of Event Camera Video.

- **Aaron Smith** (2019-2021). Research Topic: Receiver Driven Video Distribution.
- **Ziqiao Zhou** (2018-2020). Research Topic: Information Leakage in Computation.
- **Dave Estes** (2012-2020). Research Topic: The n-Dimensional Display Interface.
- **Kishore Rathinavel** (2018-2020). Research Topic: Foveated and Volumetric See-Through Near-Eye Displays.
- **David Dunn** (2017-2019). Research Topic: Optical-See-Through Displays for Augmented Reality.
- **Alex Blate** (2015-2019). Research Topic: Low-Latency Tracking for Augmented-Reality Systems.
- **Peter Lincoln** (2014-2018). Research Topic: Low-Latency Augmented-Reality Displays.
- **Sridutt Bhalachandra** (2016-2018). Research Topic: Using Runtime Energy Optimizations to Improve Energy Efficiency in High Performance Computing.
- **Mukesh Agrawal** (2013-2014), Duke University. Research Topic: Testing Many-Core System-on-Chip Designs.
- **Bipasa Chattopadhyay** (2014-2015). Research Topic: Incorporating pragmatic constraints and behaviors in real-time systems.
- **Kevin Snow** (2012-2014). Research Topic: Computer Security.
- **Haohan Li** (2012-2013). Research Topic: Scheduling Mixed-Criticality Real-Time Systems.
- **Jinghe Zhang** (2011-2013). Research topic: Uncertainty Analysis in Large-Scale State Estimation With Applications in Power Systems.
- **John Hansen** (Fall 2005-Spring 2012), see above.
- **Jeff Pool** (Fall 2007-Spring 2012), see above.
- **Justin Hensley** (Fall 2003-Fall 2006), see above.
- **Gennette Gill** (Fall 2003-Spring 2010), see above.
- **Lara Oliver** (Fall 2006), Duke University.
- **Sudarshan Bahukudumbi** (Spring 2007), Duke University.
- **Mukesh Agrawal** (Spring 2013), Duke University

OTHER GRADUATE STUDENTS SUPERVISED

- Todd Gamblin (Fall 2003-Spring 2004).
- Sushant Rewaskar (Fall 2002-Spring 2003).
- Michael Rooney (Fall 2013-Fall 2014). Research topic: High-dynamic-range image sensors.

GRANTS and other RESEARCH SUPPORT

External Funding

- (Pending final decision) NSF X-Labs: *"ASINT: Asynchronous Intensity Sensing Across Unbounded Dynamic Range and Nanosecond Timescales."* PI (joint with Prof. Ketan Mayer-Patel of UNC and Prof. Andrew C. Freeman of Baylor University). Proposal submitted June 2026, cleared first-round review, invited for oral presentation August 2026. Currently waiting for final decision. Amount applied for: $1.5M (for Phase 1).

  This project aims to build an event camera sensor in silicon, and develop a complete software stack for representation, compression, streaming, and applications of frameless event images and videos. The scope of Phase 1 is a first prototype sensor chip's layout and initial software tools. If Phase 1 is successful, Phase 2 and 3 would involve full silicon implementation of a full-resolution image sensor along with the full software stack.

- Department of Defense (Prime Sponsor), via Laboratory for Analytical Sciences (LAS) North Carolina State University subcontract: *"Analyst-Driven Rate Adaptation for Triaging Full Motion Video on the Edge,"* Lead PI (joint with PI Prof. Ketan Mayer-Patel), Jan 2024-December 2024, $75K.

  We propose a system for minimizing the bandwidth and computational requirements for an analyst to triage surveillance video. We build upon our previous LAS work in event-based video representations to move towards a fully end-to-end video pipeline where the user and application are given full control over the video bit rate.

- Department of Defense (Prime Sponsor), via Laboratory for Analytical Sciences (LAS) North Carolina State University subcontract: *"Content-Adaptive Rate Control for Surveillance Video with Event Cameras,"* Lead PI (joint with PI Prof. Ketan Mayer-Patel), Jan 2023-December 2023, $132K.

  We propose a novel system for capturing and analyzing extremely high-rate, high dynamic range surveillance video in an efficient, rate-controlled manner. We build upon our previous LAS work in video object detection, which leverages an asynchronous video representation layer to directly encode motion information in the image representation.

- Department of Defense (Prime Sponsor), via Laboratory for Analytical Sciences (LAS) North Carolina State University subcontract: *"Lightweight, Bio-inspired Triage of Video from Motion Events,"* PI (joint with Lead PI Prof. Ketan Mayer-Patel), Jan 2022-December 2022, $121K.

  We propose a novel system for casting video data into an asynchronous event-based representation to aid in motion characterization and spatio-temporal feature extraction. Our proposed system presents analysts with summary information about the amount and types of motion in lengthy surveillance videos, automatically classify objects of interest according to their motion patterns, and provide a visual interface and video client for analysts to triage both the temporal periods of interest and the spatio-temporal regions of interest in a collection of such videos.

- NSF infrastructure grant: *"II-New: Seeing the Future: Ubiquitous Computing in EyeGlasses,"* co-PI (listed as senior personnel due to limit on number of co-PIs) (PI: Prof. Jan-Michael Frahm), August 2014-July 2020, $613K.

  This project provided hardware to enable research in developing technologies for personal AR systems that are unencumbered, ubiquitous, and can be used hands-free, with a wide field-of-view display overlaid to the user's view of the surroundings.

- NVIDIA gift, August 2014, $4K.

- NSF: *"SDCI Sec: New Software Platforms for Supporting Network-wide Detection of Code Injection Attacks,"* co-PI (PI: Prof. Fabian Monrose), August 2011-July 2014, $800K.

  In this project, we developed a software platform that will enable real-time monitoring of network traffic to detect malware attacks. My role in this project was to use knowledge of instruction-set architectures (i.e., knowledge of the design of microprocessors) to prune the search space of possible locations of malware in memory, thereby speeding up detection of attacks.

- NSF: *"Power-Aware Graphics Hardware,"* co-PI (PI: Prof. Anselmo Lastra), June 2007-May 2010 (extended till May 2012), $350K.

  In this project, we investigated several approaches to reducing energy consumption in graphics processing units (GPUs). A key idea explored was to reduce the computational precision with which a scene is rendered, so as to conserve energy. We found that, for the small displays of mobile devices, precision can be reduced to yield significant energy savings without any loss of image quality. This work has potential applications in mobile hand-held applications (e.g., cell phones, personal digital assistants, game consoles, etc.), in which battery life is critical.

- DARPA: *"High-Speed Clockless Pipeline Design Flow,"* PI (subcontract via Boeing), under the CLASS program ("Clockless Logic Analysis, Synthesis, and Systems"), March 2005-March 2007. UNC share: $275K (total: $11M).

  I was part of a multi-group team, led by Boeing, which was awarded the largest grant in asynchronous design in the U.S. awarded until then. There were over twenty proposals, and only one team was successful. I was invited to the join the program for Phases 2 and 3 in order to fill a critical need. My group played the crucial role of developing an automated high-speed pipeline synthesis flow, building upon my research in high-speed asynchronous pipeline circuits. Our contribution became the single high-speed design option for the entire program. In collaboration with Handshake Solutions (a Philips spin-off), we successfully developed a new experimental high-speed pipeline design flow based on their Haste flow.

- IBM: *"Design of Latency-Insensitive Systems,"* PI (IBM Faculty Award), August 2004-July 2005, $20K.

Internal Funding

- UNC: University Research Council Research Grant, December 2010, $3,424.

- UNC: Junior Faculty Development Award, December 2002, $5,000.

- UNC: University Research Council Research Grant, December 2002, $2,300.

Other External Funding: Awards for My Students

I have worked aggressively with my students to compete for and obtain several fellowships for them, which has helped augment my extramural research funding. (The fellowship amounts listed below are not subject to overheads.)

- NSF Graduate Fellowship: Gennette Gill, Mar 2004. Approx. $40K/year for 3 years = $120K.

- UNC Dept. of Computer Science Alumni Fellowship for Dissertation Completion: Gennette Gill, August 2009. Approx. $15K (support for one semester).

- Dept. of Defense Graduate Fellowship (NDSEG): Gennette Gill, April 2004. Approx. $40K/year for 3 years = $120K.

- ATI Graduate Fellowship: Justin Hensley, May 2004. Approx. $25/year for 2 years = $50K.

- NSF East-Asia Summer Fellowship: Todd Gamblin, Feb 2004. Approx. $10K.

PROFESSIONAL SERVICE

JOURNAL EDITING

- **Guest Co-Editor, ACM Journal on Emerging Technologies in Computing Systems (JETC),** special issue on asynchrony in system design, vol. 7, no. 4, December 2011.
- **Guest Co-Editor, IEEE Design & Test of Computers (D&T),** special issue on asynchronous design, vol. 28, no. 5, September/October 2011.

CONFERENCE ACTIVITIES

- **Steering Committee Chair,** *International Symposium on Asynchronous Circuits and Systems (ASYNC).* 2016-2026.
- **Program Committee Co-Chair,** *18th International Symposium on Asynchronous Circuits and Systems (ASYNC-12),* Lyngby, Denmark, May 2012.
- **General Chair,** *15th International Symposium on Asynchronous Circuits and Systems (ASYNC),* Chapel Hill, NC, May 2009.
- **Steering Committee Member,** *International Symposium on Asynchronous Circuits and Systems (ASYNC).* 2007-2013.
- **Program Committee Co-Chair,** *13th International Symposium on Asynchronous Circuits and Systems (ASYNC-07),* Berkeley, CA, March 2007.
- **Program Committee Co-Chair,** *2nd International Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Design (FMGALS-05),* Verona, Italy, July 2005.
- **Publicity Co-Chair,** *12th International Symposium on Asynchronous Circuits and Systems (ASYNC-06),* Grenoble, France, March 2006.
- **Local Arrangements Co-Chair,** *11th International Symposium on Asynchronous Circuits and Systems (ASYNC-05),* New York, NY, March 2005.
- **Web Chair,** *16th International Symposium on Asynchronous Circuits and Systems (ASYNC-10),* Grenoble, France, May 2010.
- **Web Chair,** *17th International Symposium on Asynchronous Circuits and Systems (ASYNC-11),* Ithaca, NY, April 2011.
- **Publicity Chair,** *11th International Symposium on Asynchronous Circuits and Systems (ASYNC-05),* New York, NY, March 2005.
- **Invited Speakers Chair,** *9th International Symposium on Asynchronous Circuits and Systems (ASYNC-03),* Vancouver, Canada, May 2003.

TECHNICAL PROGRAM COMMITTEES

- 30th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2026
- 29th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2025
- 28th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2023
- 26th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2020
- 25th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2019
- 24th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2018
- 23rd IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2017
- 22nd IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2016
- 21st IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2015
- 20th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2014
- 19th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2013
- 18th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2012
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2011
- 17th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2011
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2010
- 16th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2010
- 14th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2008
- 13th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2007
- ACM/IEEE Design, Automation and Test in Europe (DATE), 2007
- ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2007
- IEEE International Conference on Computer Design (ICCD), 2006
- 12th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2006
- ACM/IEEE Design, Automation and Test in Europe (DATE), 2006
- ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2006
- IEEE International Conference on Computer Design (ICCD), 2005
- 2nd Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Architectures (FMGALS), 2005
- 11th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2005
- ACM/IEEE Design, Automation and Test in Europe (DATE), 2005
- ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2005

- 10th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2004
- ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2004
- 1st Workshop on Formal Methods for Globally Asynchronous Locally Synchronous Architectures (FMGALS), 2003
- 9th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2003
- 8th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2002
- ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2002

OTHER CONFERENCE ACTIVITIES

- Session Chair, "Power-Performance Optimization," 16th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2010
- Session Chair, "Optimization," ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU), 2002
- Session Chair, Keynote Session, 9th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2003
- Session Chair, "Design and Test," 10th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), 2004

GOVERNMENT REVIEW PANELS

(Dates and program names not provided to ensure confidentiality.)

- NSF proposal review panel, 2012
- NSF proposal review panel, 2008
- NSF proposal review panel, 2005
- NSF proposal review panel, 2004

JOURNAL AND CONFERENCE REFEREEING

- IEEE Design & Test of Computers
- IEEE Transactions on Circuits and Systems (TCAS)
- IEEE Transactions on Computers (TC)
- IEEE Transactions on VLSI (TVLSI)
- IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC)
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
- Design Automation Conference (DAC)
- European Solid-State Circuits Conference (ESSCIRC)
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI)
- IEEE/ACM International Workshop on Logic and Synthesis (IWLS)
- Conference on Advanced Research in VLSI (ARVLSI)

- International Conference on Computer Design (ICCD)
- IEE Proceedings
- Microprocessors and Microelectronics Journal (M&M)

INVITED TALKS

- **Nvidia Corp.,** Durham, NC: "Recent Advances in Asynchronous Design", June 2014. Host: John Poulton.
- **Duke University,** Durham, NC: "Design of Asynchronous Pipelined Systems," February 2007. Host: Prof. Krish Chakrabarty.
- **Achronix Semiconductor/Cornell University:** "Design of Asynchronous Pipelined Systems," January 2007. Host: Prof. Rajit Manohar.
- **Univ. of British Columbia**, Vancouver, Canada: "Design of Asynchronous Pipelined Systems," January 2007. Host: Prof. Mark Greenstreet.
- **IBM T. J. Watson Research Center,** Yorktown Heights, NY: "Design of Asynchronous Pipelined Systems," December 2006. Host: Dr. Jose Tierno.
- **Columbia University,** New York, NY: "Design of Asynchronous Pipelined Systems," December 2006. Host: Prof. Steven Nowick.
- **Univ. of Utah,** Salt Lake City, Utah: "Design of Asynchronous Pipelined Systems," November 2006. Hosts: Prof. Al Davis and Prof. Erik Brunvand.
- **Univ. of Southern California,** Los Angeles, CA: "Design of Asynchronous Pipelined Systems," November 2006. Host: Prof. Peter Beerel.
- **Univ. of California, Berkeley,** CA: "Design of Asynchronous Pipelined Systems," November 2006. Hosts: Dr. Marly Roncken and Dr. Ivan Sutherland.
- **Sun Microsystems Laboratories,** Mountain View, CA: "Design of Asynchronous Pipelined Systems," November 2006. Host: Dr. Jo Ebergen.
- **IBM T. J. Watson Research Center,** Yorktown Heights, NY: "Grappling with Latency in the Nanoscale Era," October 29, 2004. Host: Dr. Jose Tierno.
- **Columbia University,** New York, NY: "Challenges in Hardware Design in the Nanoscale Era," Mar 22, 2004. Host: Prof. Steven M. Nowick.
- **DARPA Clockless Logic Workshop,** San Jose, CA: "High-Level Synthesis of Asynchronous and Mixed-Timing Digital Systems," September 2003. Host: Dr. Robert Reuss.
- **University of California, Davis,** CA: "The Design of High-Speed Asynchronous Pipelines," May 4, 2001. Host: Prof. Jonathan Heritage.
- **Georgia Institute of Technology,** Atlanta, GA: "The Design of High-Speed Asynchronous Pipelines," April 2, 2001. Host: Prof. David E. Schimmel.
- **Univ. of North Carolina at Chapel Hill,** Chapel Hill, NC: "The Design of High-Speed Asynchronous Pipelines," March 26, 2001. Host: Prof. Gary Bishop.
- **Brown University,** Providence, RI: "The Design of High-Speed Asynchronous Pipelines," March 19, 2001. Host: Prof. Harvey Silverman.

- **Sun Microsystems Laboratories,** Mountain View, CA: "The Design of High-Throughput Asynchronous Pipelines," November 9, 2000. Host: Dr. Jo Ebergen.
- **Stanford University,** Palo Alto, CA: "The Design of High-Throughput Asynchronous Pipelines," November 8, 2000. Host: Prof. Mark Horowitz.
- **Stanford University,** Palo Alto, CA: "The Design of High-Throughput Asynchronous Pipelines," November 8, 2000. Host: Prof. Edward McCluskey.
- **IBM T. J. Watson Research Center,** Yorktown Heights, NY: "High-Throughput Asynchronous Pipelines for Fine-Grain Dynamic Datapaths," May 24, 2000. Host: Dr. Jose Tierno.
- **Theseus Logic,** Orlando, FL: "High-Throughput Asynchronous Pipelines for Fine-Grain Dynamic Datapaths," April 26, 2000. Hosts: David Lamb and Karl Fant.

TECHNOLOGY TRANSFER

- **IBM T.J. Watson Research Center:** *Design of a to-spec digital FIR filter chip for disk drives* (2000-2002).

  I was invited by IBM Research in August 2000 to apply one of my pipeline styles (the "high-capacity" style) to a real-world application: a to-spec design of an FIR filter chip for use in disk drives. The design was fabricated in silicon (0.18 micron), and the resulting chip exceeded performance goals, offering a 50% reduction in latency and 25% improvement in throughput (1.3 Giga samples/sec) over IBM's best synchronous implementation. This design provided an industrial-strength validation of my research.

- **Boeing and Handshake Solutions (a Philips spin-off):** *Development of a high-speed pipeline synthesis flow* (2005-present).

  I was invited in 2005 to join the DARPA CLASS program, a major ($14M) initiative in asynchronous design, to transfer another of my pipeline styles (the "MOUSETRAP" style) for potential commercial use. In particular, I am leading the effort to combine the high performance of my pipeline circuits with the industrial-strength asynchronous CAD flow called Haste, developed by Handshake Solutions (a Philips spin-off). We have successfully created an experimental automated pipeline synthesis flow for high-performance system implementation. My pipeline circuits were chosen for this project because of their uniqueness in offering high performance yet ease-of-construction. Upon successful completion and commercialization, this project has the potential to impact a large number of microelectronic companies by making asynchronous design technology available for large-scale industrial use.

UNC SERVICE

DEPARTMENT ADMINISTRATION

- Associate Chair for Academic Affairs (August 2023-present)

DEPARTMENT COMMITTEES

- Member, Executive Council (2024-present)
- Member, Graduate Studies Committee (2022-present)
- Member, BS/MS Academic Advising Committee (2022-present)
- Chair, Facilities and Web Committee (2009-2020)
- Member, Graduate Curriculum and Planning Committee, CAPCOM (2021-2022)
- Member, Graduate Admissions Committee (2002-2021)
- Acting Co-Chair (with Prof. K. Mayer-Patel), Graduate Admissions Committee (2017)
- Ad-Hoc Qualifying Exam Restructuring Committee (Spring 2003)
- Ad-Hoc Undergraduate Hardware Curriculum Committee (Fall 2002)

CAMPUS COMMITTEES

- Member, University Teaching Awards Committee (2026-2027)
- Member, Provost's Workshop on Liberal Arts Engineering (2026-2027)
- Member, Conflicts of Interest Committee (2012-2026)

CAMPUS MENTORING ACTIVITIES

- Faculty advisor to Computer Science Students Association (CSSA), the CS graduate student organization: Fall 2026-present.
- Faculty advisor to Bhangra Elite, a campus South-Asian nationally-competitive dance team: Fall 2004-present.
- Faculty advisor to Sikh Student Association, a campus student group: Fall 2025-present.
- Faculty advisor to Tamasha, a campus South-Asian cultural and outreach organization: Fall 2005-Fall 2006.
- UNC's ACM Programming Competition team co-coach (joint with Prof. Kevin Jeffay): Fall 2003.