

The UNIVERSITY of NORTH CAROLINA at CHAPEL HILL

Comp 411 Computer Organization

Fall 2009

Problem Set #7 [LAST ONE]

Issued Monday 11/30/09; Due Monday 12/07/09

Problem 1: Pipelining (68 points)

a) [15 points] Below is a listing by stage of the latency in a *five-stage pipelined MIPS processor*. Fill in the empty cells with the maximum instruction latency (ps) and speed (GHz) for each case.

FETCH	DECODE	EXE	MEM	WB	MAX INSTR. LATENCY (ps)	PROCESSOR SPEED (GHz)
400ps	400ps	400ps	400ps	400ps		
400ps	100ps	400ps	400ps	300ps		
100ps	100ps	500ps	100ps	100ps		
500ps	500ps	500ps	500ps	500ps		
200ps	100ps	250ps	250ps	200ps		

b) [2 points] Real pipelining isn't entirely perfect; the process introduces some latency overhead for each stage in the pipeline. Does this overhead affect overall instruction latency, throughput, or both?

Answer:

c) [6 points] Assume a five-stage MIPS processor *with standard data forwarding paths* (as discussed in class). In the two fragments below, circle the *first* instruction (if any) that will be stalled while waiting for another instruction, in spite of data forwarding being available.

1: sub \$t1, \$t2, \$t3

add \$t4, \$t2, \$t1

lw \$t5, 20(\$t4)

sub \$t6, \$t5, \$t1

2: add \$t1, \$t2, \$t3

sub \$t4, \$t2, \$t1

lw \$t5, 20(\$t1)

lw \$t6, 20(\$t5)

Problem 1: Pipelining (continued)

d) [12 points] Classify the dependencies for the following code as WAR (write after read), WAW (write after write), or RAW (read after write).

1: add \$t1, \$t2, \$t3
 add \$t6, \$t2, \$t1

Answer:

2: add \$t1, \$t2, \$t3
 add \$t2, \$t5, \$t5

Answer:

3: add \$t1, \$t2, \$t3
 add \$t1, \$t5, \$t4

Answer:

4: add \$t5, \$t2, \$t3
 add \$t1, \$t5, \$t3

Answer:

e) [4 points] In which of the code snippets in part (d) above (#1-#4) can the dependencies be resolved by renaming registers appropriately (i.e., using different registers)?

Answer:

f) [21 points] For the code fragment below, indicate in the table which registers are read and which register is written during each cycle of execution. Assume the first instruction is fetched in Cycle #1.

add \$t3, \$t2, \$t1
 add \$t6, \$t5, \$t4
 add \$t3, \$t2, \$t7
 add \$t5, \$t4, \$t3
 add \$t2, \$t6, \$t6

CYCLE	READ	READ	WRITTEN
1			
2			
3			
4			
5			
6			
7			

g) [4 points] Assume we have a program that consists of 1000 instructions in the repeated sequence `lw,sub,lw,sub...`. Each instruction depends on the result of the immediately previous instruction. If the program is executed on a five-stage pipelined MIPS processor with data forwarding, what would the actual CPI be?

Answer:

f) [4 points] If there were no forwarding in the scenario above, what would the CPI be?

Answer:

Problem 2: Memory (2 points for each part = 32 points)

Rate the spatial and temporal localities of the following scenarios by writing in “high” or “low”.

a) Listening to a full MP3 file a single time through.

Spatial:	Temporal:

b) Repeatedly editing the cells in a small spreadsheet until the numbers come out correctly.

Spatial:	Temporal:

c) Adding \$10 to the balance of every user in an online banking system. Assume the users are traversed in the order they are stored in the system (e.g. by user ID).

Spatial:	Temporal:

d) Adding \$10 to the balance of every user in an online banking system. Assume the users are traversed in a different order than they are stored in the system (e.g. by first name).

Spatial:	Temporal:

e) Repeatedly updating a single user’s account balance in an online banking system.

Spatial:	Temporal:

f) Repeatedly updating the balance of a subset of users in the order they are stored in the system.

Spatial:	Temporal:

g) for (x=0; x<100; x++)
array[x]=5;

Spatial:	Temporal:

h) for (x=0; x<100; x++)
array[0]+= x;

Spatial:	Temporal:

i) for (x=0; x<100; x++)
for (y=0;y<100;y++)
array[y]+=y;

Spatial:	Temporal:

j) for (x=0; x<100; x++)
for (y=0;y<100;y++)
array[x*1000+y]=5;

Spatial:	Temporal:

Problem 2: Memory (continued)

Your company is building a new system for a customer and they have tasked you with determining whether this system should use a write-through (**WT**) or write-back (**WB**) cache. Give your choices for each scenario below and **explain** why.

k) The customer asks for the highest performance machine possible.

Answer:
 Why?:

l) The customer is concerned primarily with data integrity rather than speed.

Answer:
 Why?:

m) The customer's intended use is for rapid, real-time response to wind variation on an airplane.

Answer:
 Why?:

n) The customer is major hospital planning on logging patient's medicine dosage only for statistical information.

Answer:
 Why?:

o) The customer is an ER recording patient's medicine dosage and using your system as their primary system.

Answer:
 Why?:

p) The customer is just a general user.

Answer:
 Why?: