The UNIVERSITY *of* NORTH CAROLINA *at* CHAPEL HILL

Comp 411 Computer Organization
Fall 2012
Prof. Montek Singh

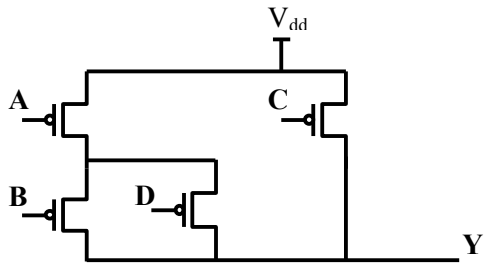
Exam #2: SAMPLE QUESTIONS
(The actual exam will have 13-18 questions.)

1. (3 points) Show the transistor-level diagram of a *single* CMOS logic gate that implements a 3-input NOR function, i.e., $F = \overline{A + B + C}$.

(1 point) Complete the corresponding truth table on the right.

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

2. (3 points) Show the complementary set of transistors that complete the following CMOS gate:



(1 point) Which Boolean expression is implemented by this circuit?

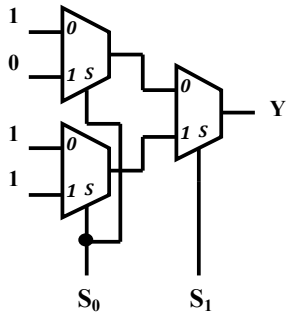
Answer: Y = _____

3. (2 points) For the Boolean function described by the truth table on the right, write down the corresponding *sum-of-products* Boolean expression.

X	Y	Z
1	1	0
0	1	1
1	0	1
0	0	0

Answer: $Z =$ _____

4. (1 points) On the right is a circuit made up of 2-to-1 multiplexers. Give the values of S_0 and S_1 for which the output Y is *zero.*



Answer: _____

(1 point) Give a Boolean equation for Y or for $\overline{Y}$ (your choice) in terms of S_0 and S_1.

Answer: ___ = _____

5. (3 points) Suppose we want to multiply two large numbers, each up to 512 bits wide. We are looking at implementing a 512-bit simple combinational multiplier (along the lines of Lecture 13 Slide 11). If someone tells us that a 16-bit simple combinational multiplier has a worst-case propagation delay of 200 nanoseconds, calculate the worst-case propagation delay of the 512-bit design.

Answer: _____

6. (2 points) When checking the equality of two *unsigned* numbers, $A == B?$, which (one or more) of the following flags need to be checked: *Z, N, C, V?*

Answer: _____

7. (1 point) Suppose you wanted to set certain bits of an operand to 1, while keeping the remaining ones as they are. Which of the following logical operations would you use: AND, OR, XOR, NOR?

   Answer: _____

8. (2 points) Can the number 9/5 be *exactly* represented by an IEEE single-precision floating-point number? Briefly explain your answer.

9. (2 points) Suppose two single-precision floating-point numbers are multiplied, with E field (exponent + bias) values of 50 and 45 respectively. What can you say about the value of the E field of the result?

10. (1 point) How is the number *zero* represented in IEEE single-precision floating-point?

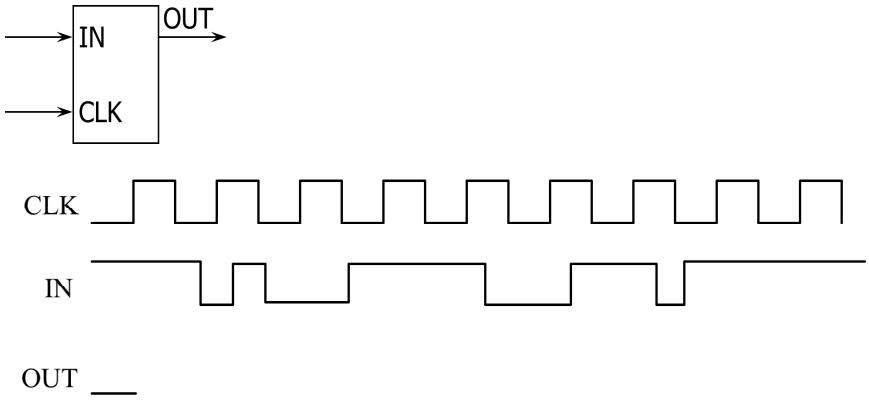
11. (1 point) Alice buys a game console that is advertised as having a speed of 1500 MIPS. Bob buys a game console that is advertised with a speed of 1000 MIPS. Briefly describe a scenario in which Bob's device is faster than Alice's.

12. (3 points) In a certain set of benchmark programs about every 5^{th} instruction is a floating-point instruction that takes 9 clock cycles to execute. The CPI for all other instructions is 4 clock cycles. What is the runtime for a program that executes 2 billion instructions if the computer runs on a 1 GHz clock?

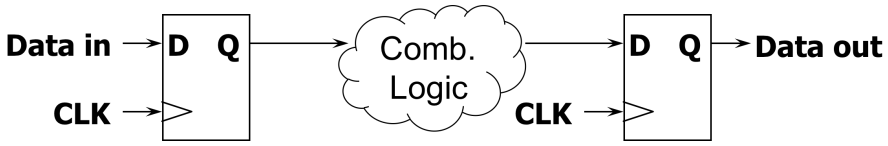
13. (2 points) Suppose a program containing 1 million instructions has an average CPI of 2.0, and runs on Machine A in 2 seconds. Next, it is recompiled to run on another computer, Machine B, which has the same clock speed as Machine A, but otherwise has a very different architecture and a different instruction set. If the CPI of the program is 1.0 on Machine B, how long does it take to finish execution on Machine B?

    a. 2 seconds
    b. 1 second
    c. 4 seconds
    d. 0.5 second
    e. Insufficient information

14. (3 points) Refer to the following picture of a latch (not an edge-triggered flipflop, but a simple positive static D latch). For the input waveforms shown for CLK and IN, draw the output waveform for OUT. Assume that setup/hold times and propagation delay are negligible.



15. (3 points) Refer to the following circuit. Suppose the propagation delay of each flipflop is 1 ns (i.e., the delay from the up-transition of the clock to the data appearing at the flipflop's output), and suppose that the setup time for each flipflop is also 1 ns, and the hold time is zero.



If the latency (i.e., worst-case propagation delay) of the block of combinational logic is 8 ns, how fast can the clock be run?

[There will be 13-18 questions on the actual exam.]