

*The UNIVERSITY of NORTH CAROLINA at CHAPEL HILL*

**Comp 411 Computer Organization**

Fall 2012

**Problem Set #5 [LAST ONE]**

*Issued Monday, 11/26/12; Due Friday, 11/30/12  
(either hand in your work during the lab hour,  
or under the TAs' doors [SN045 or SN343] by midnight)*

**Problem 1. Performance (60 points)**

Consider five different processors, P1, P2, P3, P4 and P5 executing the *same instruction set* with the clock rates and CPIs given below:

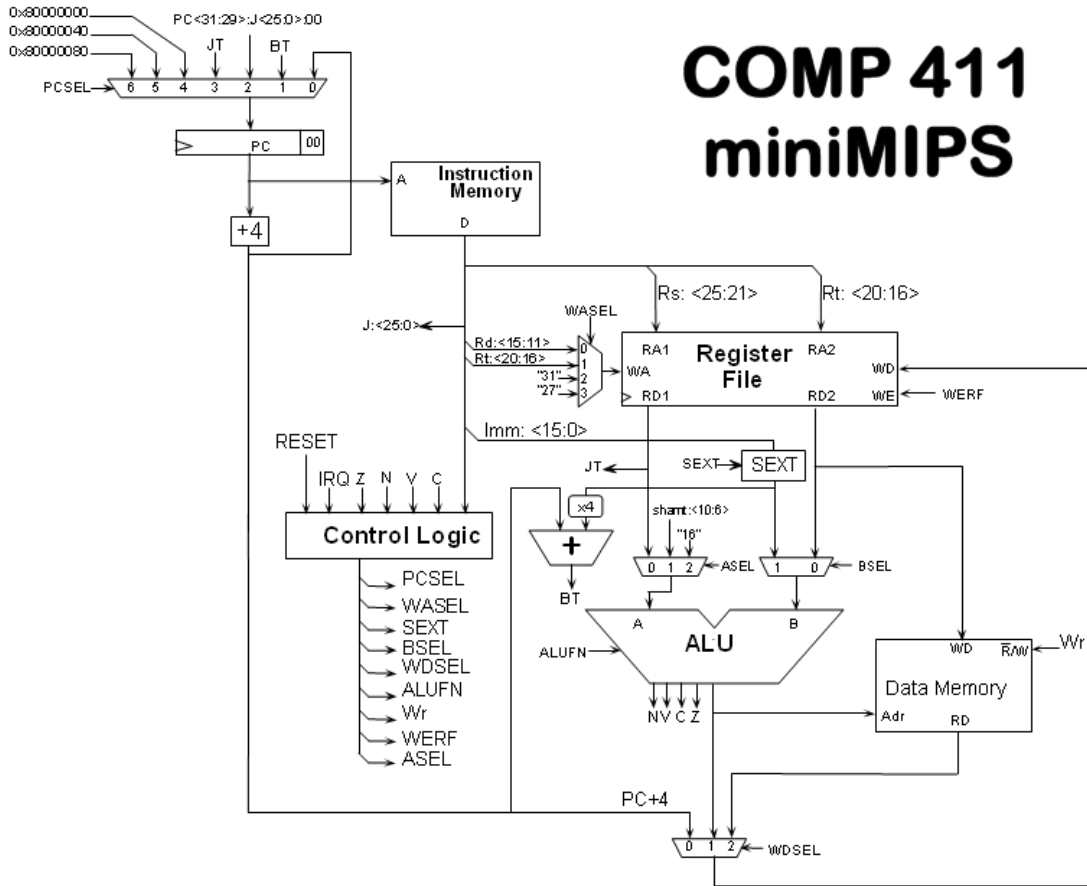
<i>Processor</i>	<i>Clock Rate</i>	<i>CPI</i>
P1	3.0 GHz	1.5
P2	2.5 GHz	1.0
P3	4.0 GHz	2.2
P4	1.0 GHz	1.0
P5	5.0 GHz	3.0

- a) [15 points] Which processor has the highest performance as expressed in instructions per second? (First, write the formula for performance in terms of the quantities in the table. Then, compute the performance of each processor. Do all work in the space provided.)

- b) [30 points] Suppose each processor is given a program that runs in 10 seconds. For each processor, determine the number of clock cycles corresponding to this time, and the number of instructions executed in this time. (Again, show the generic equation for clock cycles and instruction count first, then the calculation for each processor.)
- c) [15 points] Suppose now that we are trying to reduce the execution time for each of the processors by 30%, but this leads to an increase of 20% in each processor's CPI. What clock rates should the processors be run at in order to achieve this time reduction? (Show the generic equation first, then the calculation for each processor.)

**Problem 2. “Out of Control” (40 points)**

Refer to the following picture of a MIPS implementation and answer the question below.



# COMP 411 miniMIPS

Fill in the missing entries of the Control Logic in the table below, based on the data path shown above. *Hint:* All of the information you need to answer this question can be found in the slides from Lecture #16.

Opcode	PCSEL	WASEL	SEXT	BSEL	WASEL	ALUFN				Wr	WERF	ASEL
						Sub	Bool	Shft	Math			
sub	0	0	X	0	1	1	XX	0	1	0	1	0
xor	0	0								0		
addi	0	1										
sll	0	0	X	0	1					0	1	
andi	0									0		
lw					2					0		
sw										1		
j						X	XX	X	X	0		
jal						X	XX	X	X	0		
lui										0		