The UNIVERSITY *of* NORTH CAROLINA *at* CHAPEL HILL

Comp 411 Computer Organization
Fall 2017
Prof. Montek Singh

Final Exam: SAMPLE QUESTIONS
(The actual exam will be approximately twice as long.)

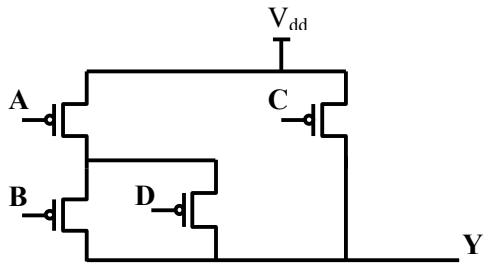
Note: These questions focus only on the post-midterm material, and not all of the material that will be on the final exam. Please use these only as rough guidance for the type of questions you can expect on the actual exam, and not as a study guide. Also, the exam will be partly or wholly answered on Sakai, which will necessitate a change in the type and number of questions.

1. (3 points) Show the transistor-level diagram of a *single* CMOS logic gate that implements a 3-input NOR function, i.e., $F = \overline{A + B + C}$.

   (1 point) Complete the corresponding truth table on the right.

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

2. (3 points) Show the complementary set of transistors that complete the following CMOS gate:



   (1 point) Which Boolean expression is implemented by this circuit?

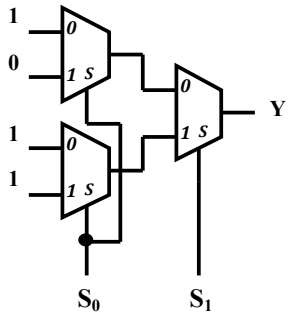
   Answer: Y = _____

3. (2 points) For the Boolean function described by the truth table on the right, write down the corresponding *sum-of-products* Boolean expression.

X	Y	Z
1	1	0
0	1	1
1	0	1
0	0	0

Answer: $Z =$ _____

4. (1 points) On the right is a circuit made up of 2-to-1 multiplexers. Give the values of S_0 and S_1 for which the output Y is *zero.*



Answer: _____

(1 point) Give a Boolean equation for Y or for $\overline{Y}$ (your choice) in terms of S_0 and S_1.

Answer: ___ = _____

5. (3 points) Suppose we want to multiply two large numbers, each up to 512 bits wide. We are looking at implementing a 512-bit simple combinational multiplier. If someone tells us that a 16-bit simple combinational multiplier has a worst-case propagation delay of 200 nanoseconds, what is the worst-case propagation delay of the 512-bit design.

Answer: _____

6. (2 points) When checking the equality of two *unsigned* numbers, *A == B?,* which (one or more) of the following flags need to be checked: *Z, N, C, V?*

Answer: _____

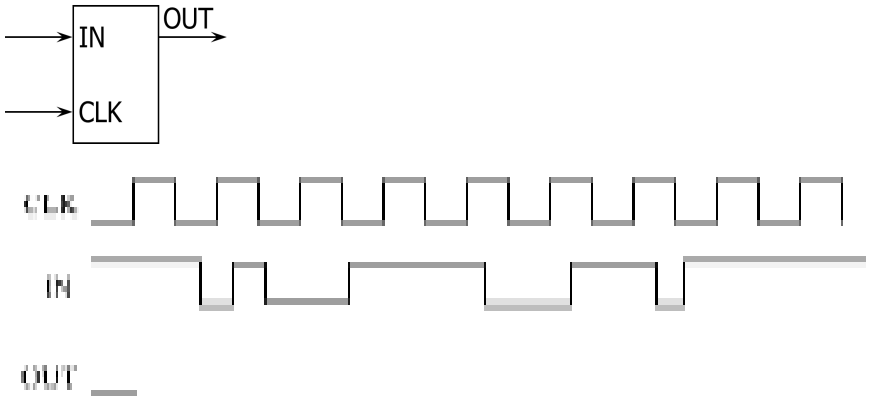
7. (1 point) Suppose you wanted to set certain bits of an operand to 1, while keeping the remaining ones as they are. Which of the following logical operations would you use: AND, OR, XOR, NOR?

   Answer: _____

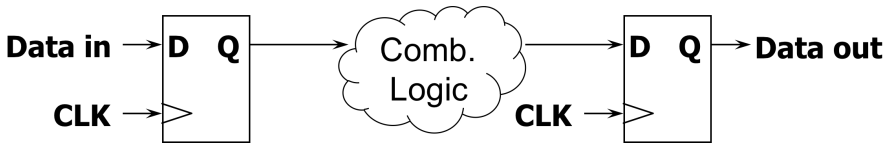
8. (2 points) Can the number 9/5 be *exactly* represented by an IEEE single-precision floating-point number? Briefly explain your answer.

9. (1 point) How is the number *zero* represented in IEEE single-precision floating-point?

10. (3 points) Refer to the following picture of a latch (not an edge-triggered flipflop, but a simple positive latch). For the input waveforms shown for CLK and IN, draw the output waveform for OUT. Assume that setup/hold times and propagation delay are negligible.



11. (3 points) Refer to the following circuit. Suppose the propagation delay of each flipflop is 1 ns (i.e., the delay from the up-transition of the clock to the data appearing at the flipflop's output), and suppose that the setup time for each flipflop is also 1 ns, and the hold time is zero.



What is the maximum latency allowable for the block of combinational logic if the clock must be run at 100 MHz?

12. (3 points) List the state of all of the control signals that the control logic must generate for the **`srav`** instruction.

PCSEL =	WASEL =
SEXT =	WDSEL =
ALUFN =	Wr =
ASEL =	BSEL =
WERF =	