*The* UNIVERSITY *of* NORTH CAROLINA *at* CHAPEL HILL

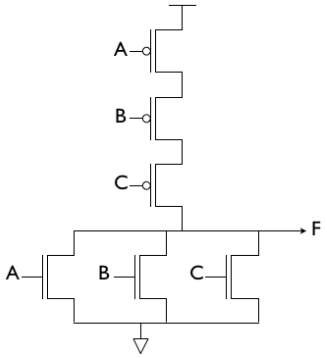
**Comp 411 Computer Organization**
Fall 2017
Prof. Montek Singh

**Final Exam: SAMPLE QUESTIONS — Solutions**
(The actual exam will be approximately twice as long.)

*Note: These questions focus only on the post-midterm material, and not all of the material that will be on the final exam. Please use these only as rough guidance for the type of questions you can expect on the actual exam, and not as a study guide. Also, the exam will be partly or wholly answered on Sakai, which will necessitate a change in the type and number of questions.*

1. (3 points) Show the transistor-level diagram of a *single* CMOS logic gate that implements a 3-input NOR function, i.e., $F = \overline{A + B + C}$.

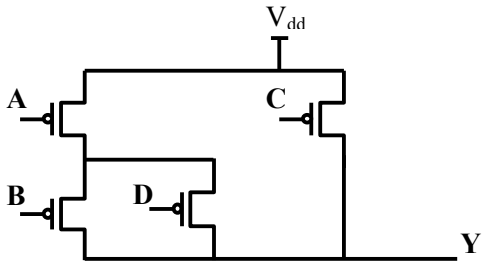
Answer:




| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

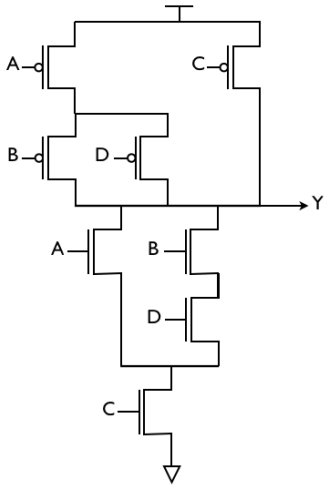
(1 point) Complete the corresponding truth table on the right.

2. (3 points) Show the complementary set of transistors that complete the following CMOS gate:




(1 point) Which Boolean expression is implemented by this circuit?

Answer: The circuit diagram is shown on the right. Its Boolean equation is easily inferred from the p-transistor network as $Y = \bar{A}(\bar{B} + \bar{D}) + \bar{C}$. Alternatively, the equation can also be inferred from the n-transistor network as $Y = \overline{(A + BD)C}$.

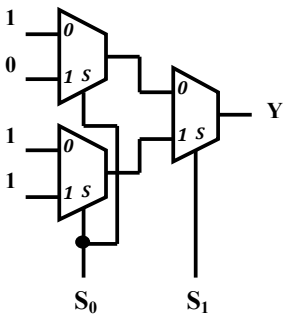



3. (2 points) For the Boolean function described by the truth table on the right, write down the corresponding *sum-of-products* Boolean expression.

| X | Y | Z |
|---|---|---|
| 1 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 0 | 0 | 0 |

Answer: $Z = \bar{X}Y + X\bar{Y}$

4. (1 points) On the right is a circuit made up of 2-to-1 multiplexers. Give the values of $S_0$ and $S_1$ for which the output <u>*Y* is *zero.*</u>




Answer: $S_0 = 1,\ S_1 = 0$

(1 point) Give a Boolean equation for *Y* or for $\bar{Y}$ (your choice) in terms of $S_0$ and $S_1$.

Answer: Since Y is 0 only when $S_0$=1 and $S_1$=0, therefore, $\bar{Y} = S_0\bar{S_1}$. Alternatively, Y is 1 for the remaining three combinations of inputs, so $Y = \overline{S_0}\,\overline{S_1} + \overline{S_0}S_1 + S_0S_1$.

5. (3 points) Suppose we want to multiply two large numbers, each up to 512 bits wide. We are looking at implementing a 512-bit simple combinational multiplier. If someone tells us that a 16-bit simple combinational multiplier has a worst-case propagation delay of 200 nanoseconds, what is the worst-case propagation delay of the 512-bit design.

Answer: Since the delay of a combinational multiplier is proportional to the number of bits in the operands, the delay of the 512-bit design is 32 times the delay of the 16-bit design, therefore 200 * 32 ns = 6.4 microseconds.

6. (2 points) When checking the equality of two *unsigned* numbers, *A == B?,* which (one or more) of the following flags need to be checked: *Z, N, C, V?*

   Answer: To test equality, whether the numbers are signed or unsigned, only the Z flag needs to be checked. (For equality/inequality testing, it does not matter if the numbers are signed or unsigned.)

7. (1 point) Suppose you wanted to set certain bits of an operand to 1, while keeping the remaining ones as they are. Which of the following logical operations would you use: AND, OR, XOR, NOR?

   Answer: OR

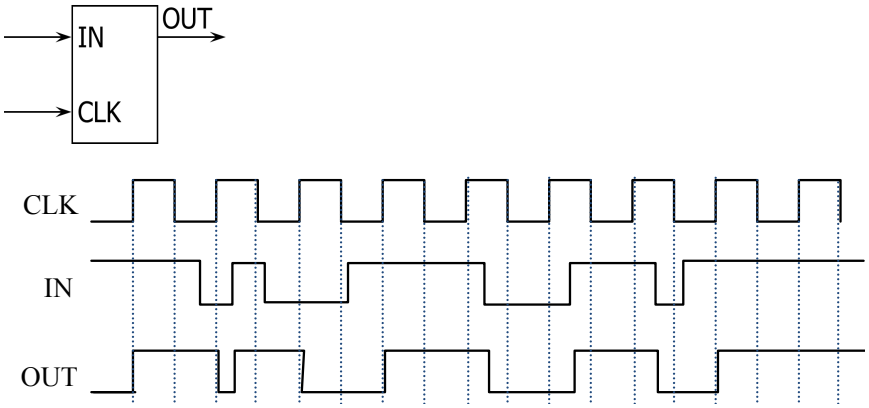
8. (2 points) Can the number 9/5 be <u>*exactly*</u> represented by an IEEE single-precision floating-point number? Briefly explain your answer.

   Answer: No. Only fractions whose denominator is a power of 2 have a finite representation in binary.

9. (1 point) How is the number *zero* represented in IEEE single-precision floating-point?

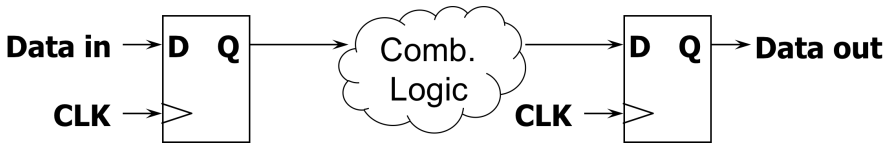
   Answer: S could be 0 or 1, E = 0, F = 0.

10. (3 points) Refer to the following picture of a latch (not an edge-triggered flipflop, but a simple positive latch). For the input waveforms shown for CLK and IN, draw the output waveform for OUT. Assume that setup/hold times and propagation delay are negligible.




   Answer: See the waveform above. The latch allows the value of IN to propagate to the output OUT only when CLK is 1. When CLK is 0, the latch remembers (or "holds") its last value when CLK was 1.

11. (3 points) Refer to the following circuit. Suppose the propagation delay of each flipflop is 1 ns (i.e., the delay from the up-transition of the clock to the data appearing at the flipflop's output), and suppose that the setup time for each flipflop is also 1 ns, and the hold time is zero.




What is the maximum latency allowable for the block of combinational logic if the clock must be run at 100 MHz?

Answer: Refer to Lecture 13, slide 37. The clock period $T_{clk}$ must be at least as long as the flipflop latency + combinational logic latency + setup time. Here, $T_{clk}$ is 1/100MHz = 10 ns. Therefore, the maximum allowable latency for the combinational logic = 10 ns – 1 ns – 1ns = 8 ns.

12. (3 points) List the state of all of the control signals that the control logic must generate for the **`srav`** instruction.

| | |
|---|---|
| PCSEL = 0 | (because we want PC = PC+4) |
| WASEL = 0 | (because value is written to Rd) |
| SEXT = X | (because sign extension does not matter; imm value not used) |
| WDSEL = 1 | (because ALU result is written to destination register) |
| ALUFN =X1110 | (code for right arithmetic shifts) |
| Wr = 0 | (because data memory is not written) |
| ASEL = 0 | (because Rs is one of the operands, i.e., the shift amount) |
| BSEL = 0 | (because Rt is the other operand, i.e., the value to be shifted) |
| WERF = 1 | (because a value is stored in the register file) |