The UNIVERSITY *of* NORTH CAROLINA *at* CHAPEL HILL

Comp 541 Digital Logic and Computer Design
Fall 2014

Quiz #3, Friday 11//14/14
20 minutes, 10 points

1) Suppose we are looking at a certain bit position in the design of an adder. When is this bit position said to *propagate* a carry (i.e., produce *P=1*), and when is it said to *generate* a carry (i.e., *G=1*)?

   Answer: P = 1 when _____

   G = 1 when _____

2) Which flag(s) does the MIPS controller need to examine to determine the outcome of a branch (beq/bne) instruction?
   Answer:

3) Which flag(s) does the MIPS ALU need to examine to determine the outcome of *less-than-unsigned* and *less-than-signed* operations? Write the Boolean expression in terms of these flag(s).

   less-than-unsigned:

   less-than-signed:

4) Give two instructions for which the value of the *RegWrite* control signal (the write enable for the register file) is '0'.
   Answer:

5) If the value of the program counter, PC, is 0x12345670, and the instruction `j 2` is executed (i.e., the value of the immediate field is '2'), then what is the new value of PC?
   Answer:

6) If the value of the program counter, PC, is 0x12345670, and the instruction `beq $0,$0,2` is executed (i.e., the value of the immediate field is '2'), then what is the new value of PC?
   Answer:

7) Suppose you have a 2^8x16 ROM. How many address bits, data bits, and memory locations does this ROM have?
   Answer:

8) Give one benefit of SRAM over DRAM, and one benefit of DRAM over SRAM (clearly identify which is which).
   Answer:

9) In one sentence, describe what is meant by *nibble* or *burst mode* of memory access?
   Answer:

10) Suppose you wanted to treat all *unimplemented* instructions in your Lab 10 MIPS (e.g., multiply) as equivalent to *no operations* (NOPs), i.e., executing them must not change the state of the processor except to increment the PC to the next instruction. In one sentence, describe how you will design your controller unit to implement this behavior.
    Answer: