Comp 541 Digital Logic and Computer Design
Fall 2014

Quiz #4, Friday 11/21/14
20 minutes, 10 points

1) List two advantages of a multi-cycle (not pipelined) MIPS processor, compared to a single-cycle implementation.
   Answer:

2) Why is it that the multi-cycle MIPS can have both the instruction and data memories combined into one memory, whereas the single-cycle MIPS had them separate?
   Answer:

3) How many clock cycles do each of the following instructions take in a multi-cycle MIPS implementation?
   - BEQ:
   - ADDI:
   - LW:
   - SW:

4) In one sentence, describe the basic idea behind memory-mapped I/O.
   Answer:

5) In one sentence each, what are spatial parallelism and temporal parallelism?
   Spatial:
   Temporal:

6) Identify all the data hazards if the following program is run on a pipelined MIPS, assuming no data forwarding:
   ```
   xor $1, $2, $3
   lw $2, 40($1)
   add $4, $1, $2
   ```

7) List one software/compiler technique and one hardware technique to addressing data hazards:
   Software:
   Hardware:

8) When is a control hazard said to have occurred?
   Answer:

9) What is branch prediction, and how does it help?
   Answer:

10) Give three examples of internal interrupts and one example of external interrupts.
    Answer: