
Exercises to be submitted: Do the following textbook exercises:

- 3.2 (5 points)
- 3.4 (5 points)
- 3.6 (5 points)
- 3.10 (9 points)
- 3.12 (7 points). Start with an SR-latch using cross-coupled NOR gates. Add AND gates to incorporate an enable signal (clock). Now make a minor change to introduce an asynchronous reset capability, i.e., the latch output must reset to '0' whenever the input R is '1', without waiting for the clock/enable to be on.
- 3.16 (6 points)
- 3.18 (8 points)
- 3.20 (5 points)
- 3.22 (20 points). Assume the state encoding: S0=00, S1=01 and S2=10. Show state transition table and output table for the FSM. Write Boolean equations (sum-of-products) for the next state and output logic. You do not have to generate optimal (i.e., minimized) Boolean equations, and you do not have to sketch a circuit schematic.
- 3.24 (20 points). Only show the following: state diagram, state encoding, state transition table, and output table. Skip Boolean expressions and circuit schematic.
- 3.28 (10 points). Draw the state diagram only (no truth tables, equations, circuits needed).