Analysis of probability and energy of nanometre CMOS circuits in presence of noise

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Motivated by the necessity to consider probabilistic approaches to future designs, probability and switching energy characteristics of probabilistic CMOS (PCMOS) circuits are analysed. Using 90 and 65 nm processes, detailed analytical models for the probability of correctness (p) of these circuits are developed and verified through circuit simulations.

Introduction: As the feature sizes of semiconductor devices decrease, their behaviour becomes increasingly 'probabilistic' owing to sources such as thermal noise [1], ground bounce [2] and process variations [3]. Enhancing the robustness of circuits and systems to this probabilistic behaviour introduces some redundancy. Thus, there is a fundamental tradeoff between robustness and energy efficiency. This tradeoff has been exploited to enable energy efficient computing platforms via probabilistic computing [4]. The basic element of this approach is a probabilistic CMOS (PCMOS) device, which is a noisy CMOS device that computes correctly with probability p. In our previous work, characterisation of a PCMOS switch [5], a method to use these switches to build probabilistic architectures [6], and the tradeoffs between energy, performance and p of this switch [7] have been studied. In this Letter, we analyse the probabilistic behaviour of larger circuits by first developing probability models of primitive gates, which are then input to a graph-based model to find the probabilities of larger circuits.

Probability and switching energy models of primitive PCMOS gates: In modelling the p of a PCMOS gate, we consider that noise is coupled to the evaluation nodes [8] that carry the logical information of the gate. For example, Fig. 1 shows the evaluation nodes of an XOR gate. In the Figure, noise sources coupled to the nodes V_{in1}, V_{in2}, V_{inv1}, V_{inv2} and V_o are V_{n1}, V_{n2}, V_{n3}, V_{n4} and V_{n5}, respectively (V_{n1} and V_{n2} not shown in the Figure). Each noise source is characterised by a zero mean Gaussian distribution and white spectrum. The standard deviation (or RMS value) of the noise due to sources V_{n1}, V_{n2}, V_{n3}, V_{n4} and V_{n5} is σ_1, σ_2, σ_3, σ_4 and σ_5, respectively, and the associated p values are p_1, p_2, p_3, p_4 and p_5. The probability of correctness value p_i for the noise RMS value of σ_i, where $i \in \{1, 2, 3, 4, 5\}$, is found from [5]:

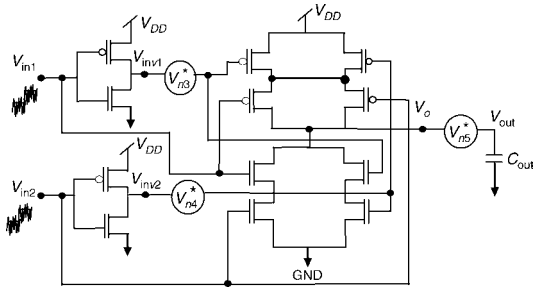

Fig. 1 *A PCMOS XOR gate coupled with noise at its evaluation nodes*

V_{in1}		V_{in2}		V_{out}	
Value	Prob.	Value	Prob.	Value	Prob.
0	p_1	0	p_2	0	$(-2p_2-2p_1+6p_1p_2)p_3^3+(3p_1+3p_2-7p_1p_2)p_3^2$ $+(1-3p_1-3p_2+4p_1p_2)p_3+p_2+p_1-p_1p_2$
0	p_1	1	p_2	1	$(2-4p_1-2p_2+6p_1p_2)p_3^3+(-3+3p_2+4p_1p_2+7p_1p_2)p_3^2$ $+(2-p_1-3p_2+4p_1p_2)p_3+p_2-p_1p_2$
1	p_1	0	p_2	1	$(2-4p_2-2p_1+6p_1p_2)p_3^3+(-3+3p_1+4p_2-7p_1p_2)p_3^2$ $+(2-p_1-3p_1+4p_1p_2)p_3+p_1-p_1p_2$
1	p_1	1	p_2	0	$(2-4p_1-4p_2+6p_1p_2)p_3^3+(-1+4p_2+4p_1-7p_1p_2)p_3^2$ $+(-1-p_1-p_2+4p_1p_2)p_3+1-p_1p_2$

Fig. 2 *Probabilistic truth table for PCMOS XOR gate*

$$p_i = 0.5 + 0.5\mathrm{erf}\left(\frac{V_{dd}}{2\sqrt{2}\sigma_i}\right) \quad (1)$$

Next, we construct a probabilistic truth table. The truth table for our example XOR gate when $\sigma_3 = \sigma_4 = \sigma_5$, and hence $p_3 = p_4 = p_5$ is shown in Fig. 2. This truth table is derived considering all possible combinations of the binary values of the signals at the evaluation nodes; however, in Fig. 2, we show only the input and output signals and their associated probabilities. Using the probability values for V_{out} in Fig. 2 and considering that every input combination is equally probable, the p of a PCMOS XOR gate is

$$\begin{aligned} p_{XOR} = {} & \frac{1}{4} + \frac{p_1}{2} + \frac{p_2}{2} - p_1p_2 + (1 - 2p_1 - 2p_2 + 4p_1p_2)p_3 \\ & + \left(-\frac{7}{4} + \frac{7}{2}p_1 + \frac{7}{2}p_2 - 7p_1p_2\right)p_3^2 \\ & + \left(\frac{3}{2} - 3p_1 - 3p_2 + 6p_1p_2\right)p_3^3 \end{aligned} \quad (2)$$

Practical systems always have a finite bandwidth. When bandlimited white noise with maximum frequency component of $1/T_n$ is applied to the input of a system having a bandwidth of $1/T_s$, and when $1/T_n > 1/T_s$, noise is filtered by the system. In this case, the RMS value of the noise observed at the output of the system is smaller than the RMS value of the noise at the input (denoted as σ), and is modelled as $\sigma\sqrt{T_n/T_s}$ [9]. Hence, for the XOR gate shown in Fig. 1, the noise due to sources V_{n1}, V_{n2}, V_{n3} and V_{n4} is limited by the filtering effect. By using the α-power law MOSFET delay model [10] to compute the propagation delay for the ith input of the XOR gate, T_{si}, we model the equivalent noise RMS value (for each noise source V_{ni}) observed at the output using

$$\begin{aligned} \sigma_{eq}(i) &= \sigma_i\sqrt{T_{ni}/T_{si}} \\ &= \sigma_i\left(T_{ni}\Big/\left(K_{1i}T_{ni} + K_{2i}\frac{V_{dd}}{(V_{dd}-V_{th})^{\alpha}}\right)\right)^{0.5} \end{aligned} \quad (3)$$

where T_{ni} is the reciprocal of the maximum frequency component of noise with RMS value of σ_i. K_{1i} and K_{2i} are technology dependent empirical parameters fitted using HSPICE simulations. V_{th} and α are the threshold voltage and velocity saturation index parameters [10]. Next, for each noise source, we find the equivalent input probability $p_{eq}(i)$ by substituting σ_i in (1) with $\sigma_{eq}((i)$ found from (3). Hence, when the bandlimiting effect is considered, the p of a PCMOS XOR gate is found by substituting p_i values in (2) with their corresponding $p_{eq}(i)$ values. We note that T_{ni} is the same for all the noise sources. In simulations, noise is modelled as a piecewise linear (PWL) voltage source and T_{ni} corresponds to the time difference between each sample of the PWL. The value of T_{ni} is chosen to be 10 ps, which is smaller than the inverter delay of the 90 and 65 nm processes that we investigated.

Similarly, we find the p values for our other primitive gates (inverter, NAND and NOR) using the approach outlined for the XOR gate above. We model the switching energy consumed by a primitive gate by

$$E = 0.5C_{eff}V_{dd}^2 \quad (4)$$

where C_{eff} denotes the effective capacitance per switching.

Fig. 3 shows our analytical and simulation results for E against p of PCMOS XOR gates realised in 90 and 65 nm processes. We vary p and E values by changing the supply voltage (V_{dd}) of the circuit from 0.15 to 1 V. The RMS value of noise is varied from 0.15 to 0.25 V. We use HSPICE to perform circuit simulations and Matlab to generate noise sources with a Gaussian distribution. Fig. 3 shows that simulation and analytical results follow each other closely for both processes. Furthermore, for a fixed RMS value of noise, E increases as p increases and the rate of increase in E grows as p approaches 1. Hence, in the vicinity of $p = 1$, significant decrease in E can be achieved by a small reduction in p. Comparing Figs. 3*a* and *b*, we observe that, for fixed values of noise RMS and p, the XOR gate in 65 nm process has a lower E than the XOR gate in 90 nm process (for example, the points denoted by C and D in the figure). This difference is due to the lower capacitances for the 65 nm process. Thus, as the feature sizes decrease, the switching energy investment to realise a specific value of p decreases.

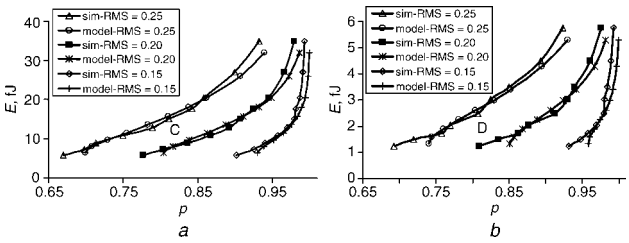

Fig. 3 *Energy-probability characteristics of a PCMOS XOR gate*

a 90 nm process
b 65 nm process

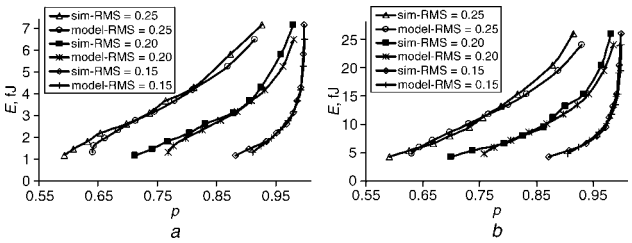

Fig. 4 *Energy-probability characteristics*

a 4-bit parity circuit
b Inverter chain circuit

Algorithm to find probability of PCMOS circuits: Given a combinational circuit with k inputs and n outputs, this algorithm finds the p values at the outputs of the circuit. The circuit is mapped to primitive gates and modelled as a directed graph $G = (V, E, m, w)$, where V is the set of primitive gates in the circuit and E is the set of directed edges connecting these gates. Edge e_{ij} represents a connection from gate v_i to gate v_j. $m(i)$ is a positive integer identifying the probability model for the gate v_i, since we use four primitive gates, $1 \leq m(i) \leq 4$, and w_{ij} is the p value for the signal represented by edge e_{ij}. P(w_{ji}) denotes the set of the probabilities of the incoming edges of v_i. We first topologically order the gates so that the probabilities are propagated in the correct order, and then visit each gate in this order. For each node v_i visited, we compute the p value at the output of the gate (pr(v_i)). In doing so, we first find the RMS values of the noise associated with each element of P(w_{ji}) using (1). Then, using (3) and (1), we find the p_{eq} value for each input of the gate. pr(v_i) is then computed using these p_{eq} values and the corresponding probability equation derived from the truth table of the gate. Next, the probabilities associated with each outgoing edge of v_i (w_{ij}) are assigned to pr(v_i). If v_i has a primary output out_l then $p_{\text{out}}(l) = \text{pr}(v_i)$.

We have tested our algorithm for small circuits including a four-bit parity circuit—a series of three XOR gates, and a chain of five inverters. Fig. 4 shows the analytical and simulation results for these circuits implemented in a 90 nm process. The average difference between the analytical and simulated p values is 0.5% for the parity circuit and 0.54% for the inverter chain. The analytical model results deviate the most from the simulation results when V_{dd} is low ($V_{dd} < 0.55$ V) because of the underestimation of the circuit delay by our model at low V_{dd} values.

As we move from primitive gates (Fig. 3) to larger circuits (Fig. 4), the rate of increase in E (with p) is preserved, whereas, for a fixed value of noise RMS, values of p in Fig. 4 are smaller owing to the additive and propagation effect of noise sources in larger circuits. In this context, our analysis is important for design and synthesis of probabilistic circuits to achieve a desired value of p.

Conclusions: We have shown a method to derive the energy-probability characteristics of primitive PCMOS gates and presented an algorithm to find the p of PCMOS circuits that are built using these gates. The simulation results for circuits realised in 90 and 65 nm processes have demonstrated the validity of our analytical models. Our work provides a basis for analysing probabilistic behaviour owing to noise and other perturbations in future technologies, and can be used in probabilistic design and synthesis methods to improve circuit reliability. For future work, we will explore the effect of leakage energy on our analysis and enrich our library of primitives with more complex gates.

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