

Avionics Hardware Issues

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Chih-hao Sun

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-HW
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-FPGA vs
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-PowerPC

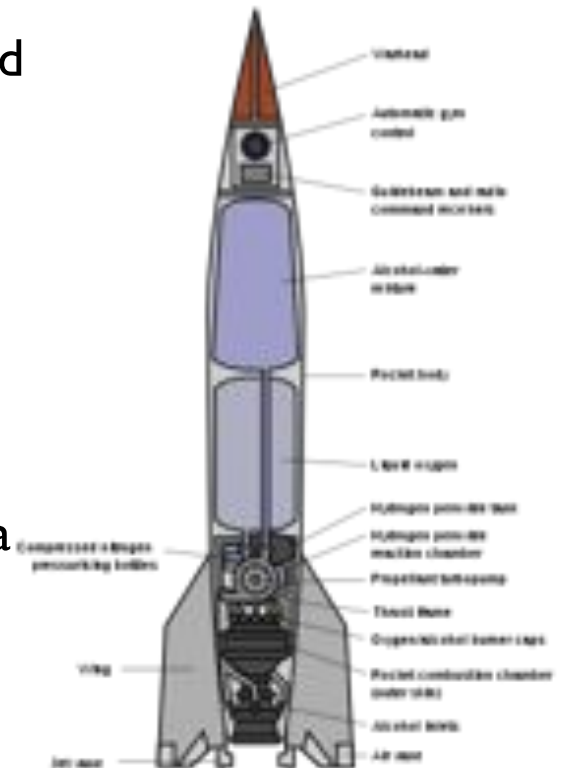
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History

- The Gyroscope, the first auto-pilot device, was introduced a decade after the Wright Brothers (1910s)
 - holds the plane level automatically
 - is connected to computers for missions(B-17 and B-29 bombers)
- German V-2 rocket(WWII) used the earliest automatic computer control system (automatic gyro control)
 - contains two free gyroscopes (a horizontal and a vertical)



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History

- Avro Canada CF-105 Arrow fighter (1958) first used analog computer to improve flyability
 - is used to reduce tendency to yaw back and forth
- F-16 (1970s) was the first operational jet fighter to use a fully-automatic analog flight control system (FLCS)
 - the rudder pedals and joysticks are connected to “Fly-by-wire” control system, and the system adjusts controls to maintain planes
 - contains three computers (for redundancy)

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History

- NASA modified Navy F-8 with digital fly-by wire system in 1972.
- MD-11 (1970s) was the first commercial aircraft to adopt computer-assisted flight control
- The Airbus A320 series, late 1980s, used the first fully-digital fly-by-wire controls in a commercial airliner
 - incorporates “flight envelope protection”
 - calculates that flight envelope (and adds a margin of safety) and uses this information to stop pilots from making aircraft outside that flight envelope.
- Boeing followed with Boeing 777 (mid-90s) as a fully-digital fly-by-wire controls

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- Single board computer
- Backplane
- Mezzanine cards
- Eurocards
- Bus
 - VMEBus
 - VPX
 - CompactPCI

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Single Board Computer

- Complete computers are built on a single circuit board
 - is centered on processors, and all other features (Ram, I/O, ...) are needed on the board to be a fully-functional computer
 - is different from PC motherboard
 - motherboard and daughterboards (graphics card or other I/O controllers)
 - smaller than ATX motherboard and without slot(no plug-in cards)
 - the cost is cheaper than ATX motherboard
 - can be plugged into a backplane as a controller in a complex computing system



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Backplane

- A circuit board connects several connectors in parallel
 - is used to connect to make up a complete system
 - most common connect pin standard: PICMG
- Differentiated form motherboard
 - lack of on-board processing and storage elements
 - motherboard may include backplane
 - a backplane with a plug-in SBC is equivalent to a motherboard
- Grown from the simple IBM ISA Bus where all connects to a common bus
- Could offered as passive(without on-board processing) and active (has some on-board processing and memory buffer)



Mezzanine Card

- Provides a degree of flexibility to a host board such that a single host can be used in a variety of applications
- Makes it possible to stuff more components into a board's limited space
- Adds function or enhancements to a board to extend product life
- Example: PCI Mezzanine Board (PMB)
 - is manufactured to the IEEE P1386.1 standard
 - offers products that are compatible with PCI bus



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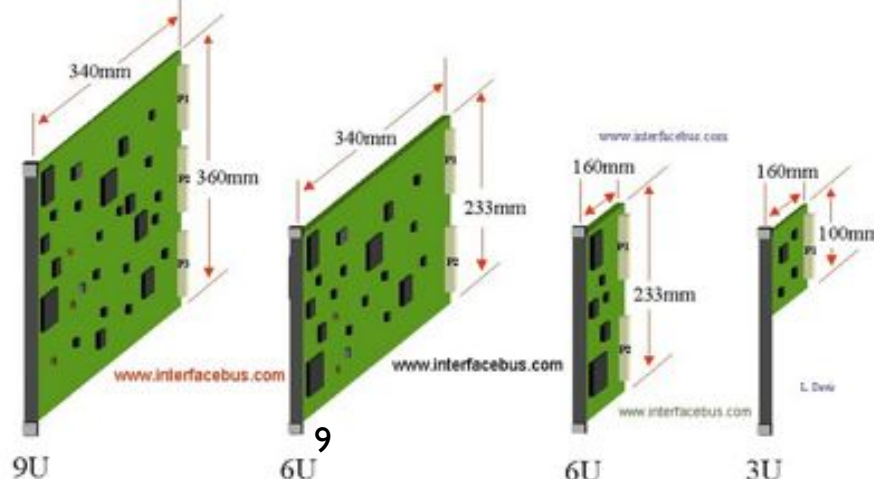
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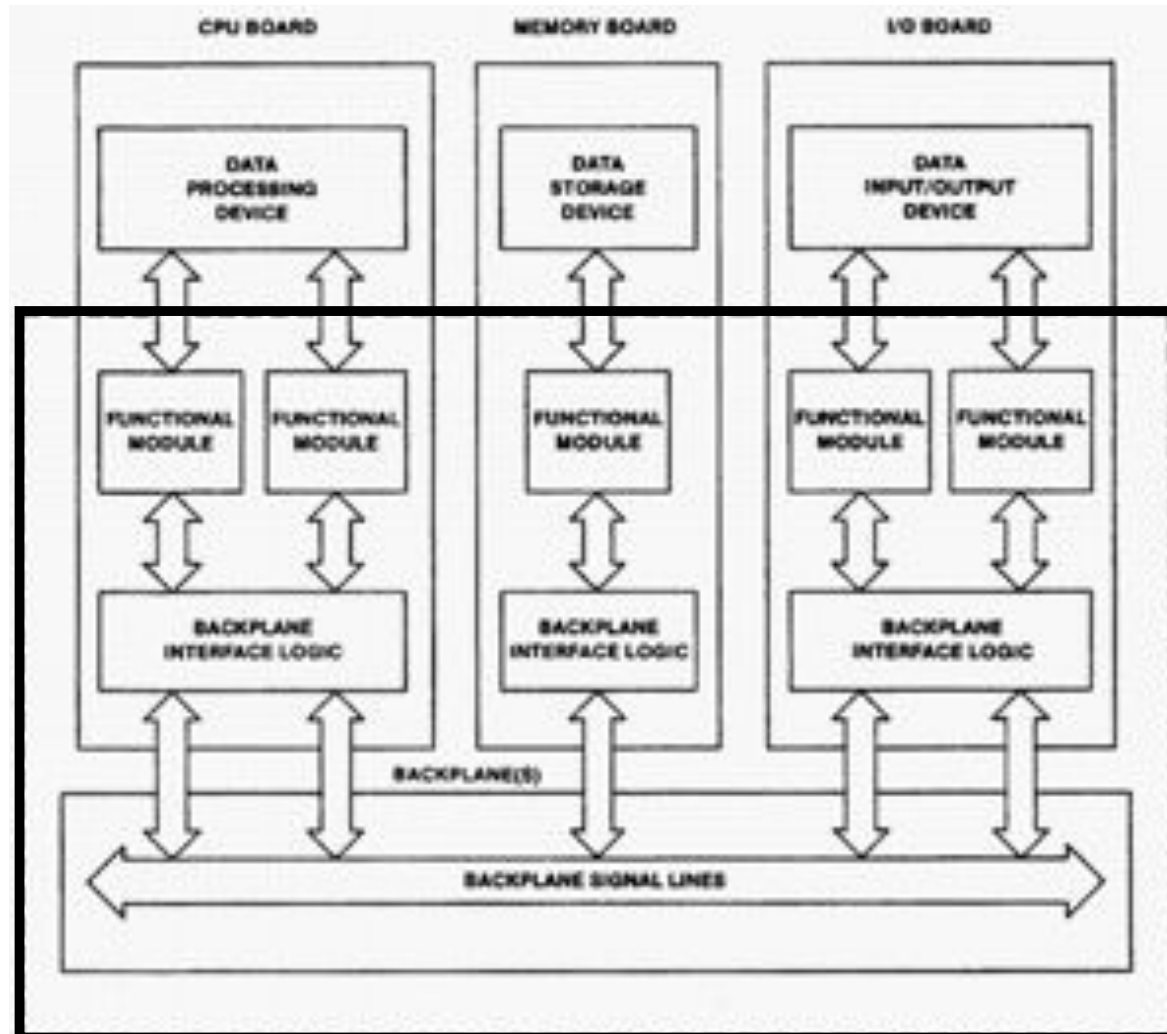
Eurocard

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- European standard format for circuit board
- Eurocard subrack's height is specified by 'U'(1.75 in'=44.45mm) unit
- Eurocard's height starts at 100 mm(3.937 in') and increments by 3U (133.350 mm(5.25in'))
 - popular height sizes:
 - 3U Eurocard is 100mm (in 3U subrack (133.35mm))
 - 6U Eurocard is 233.35mm(10.5in') (in 6U subtrack(266.70mm))
- 160 mm and 340 mm depth is popular



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VMEBus

- Developed for the Motorola 68000 line of CPUs, and standardized as ANSI/IEEE 1014-1987
- Original standard provides 8-, 16-, 32, and 64-bit(VME64,1994) parallel-bus arch., includes **data transfer, priority interrupt, arbitration, and utility**
- Two arbitration modes are supported: round-robin and prioritized
- The signaling scheme is asynchronous (don't rely on clock, need handshaking)
- Provides 7 interrupt levels to prioritize interrupts
 - is followed by the pre-defined prioritize policy in different level of interrupts
 - uses daisy chain to break the tie of two same level interrupters in the same level. (closer is winner)

VMEBus Protocol

- A module attempts to become the bus master by holding one of **Bus Request lines**(four) low
 - if two BR are low, use round-robin or other defined prioritized policy to decide which is granted.
 - if two modules hold the sam BR, a bus use daisy-chain to breaks the tie.
- After granted the bus, assert **Bus Busy**(BBSY)
- To write data, the master use **AD** and **modifier** signals to indicate the target slave and address type. Then, the master asserts **AS** and **DS** to indicate that **DATA** is ready. If data received, slave drives **DTACK**, if can't complete, drives **BERR**
- To read data, the difference are master don't pull **DS**, and slave has drives **DTACK** and **DS** if **DATA** ready

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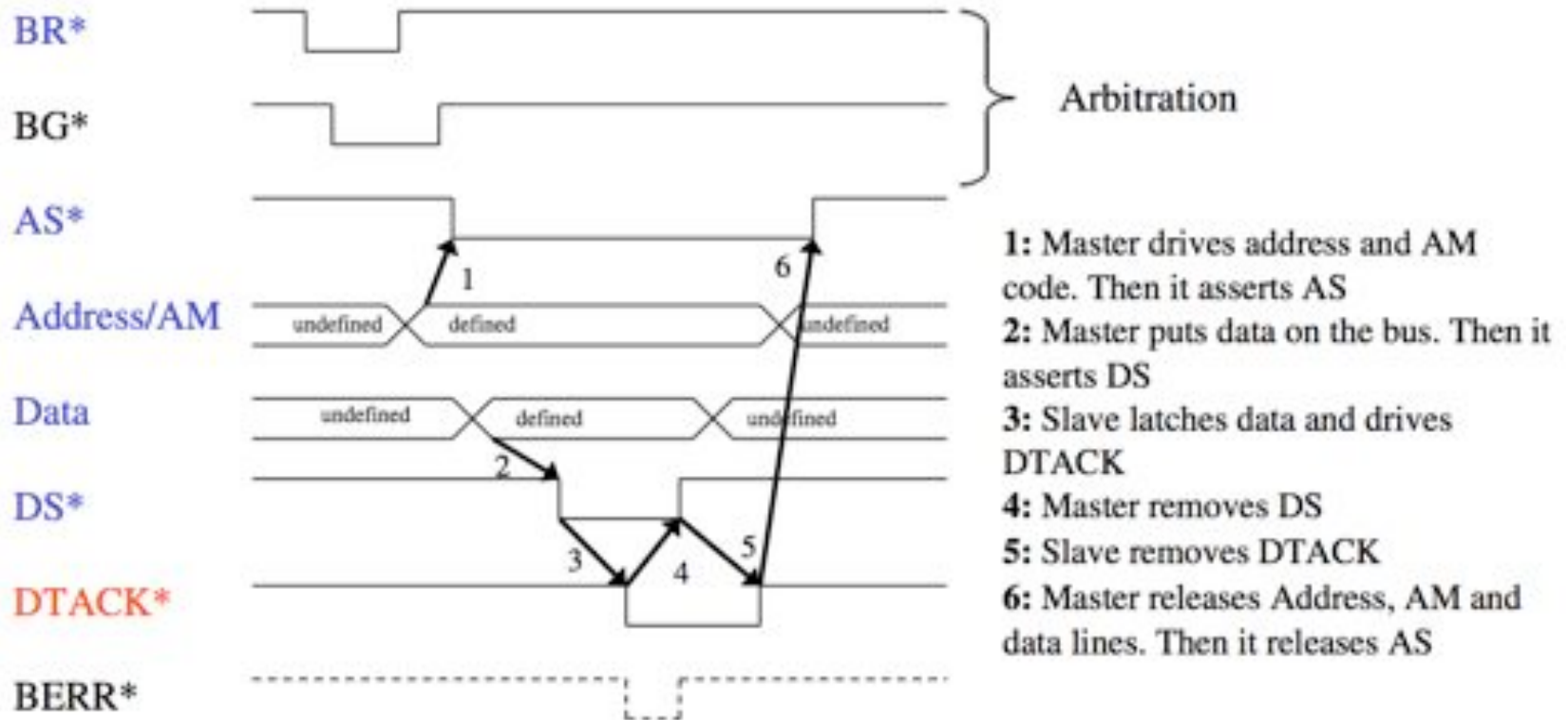
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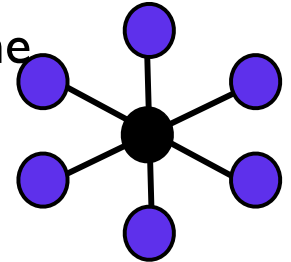
VMEBus Protocol

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Enhanced VMEbus

- VME320 is released by Arizona Digital in 1997.
 - uses “star” connection to speed up the VMEbus backplane
 - allows tighter skew delays, and speed up the system
 - new protocol called 2eSST is a synchronous protocol in which no acknowledgment is expected from the receiver of the data
 - is supported by over 103 OS running on VMEbus



UNIX Style OS	WINTel Style OS	Real Time OS
Solaris SunOS Berkeley AT&T Linux	DOS OS-2 Windows 3.1 Windows 95/98/NT	VxWorks pSOS LynxOS QNX RTLinux

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VPX

- An ANSI standard that provides VMEBus with support for high-speed serial switched fabric connect
 - supports existing high speed protocol Mezzanine Cards
 - maintains the maximum possible compatibility with VMEBus
- Differences between VMEBus
 - uses new connector, MulyiGid RT2 by Tyco Electronic
 - supports higher power specification
 - considers cooling issues.

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CompactPCI

- A system where all boards are connected via a PCI backplane
- PCI(Peripheral Component Interface) was developed in 1990
 - essentially defines a low level interface between CPU and peripheral devices
 - original PCI bus operated 33MHz to provide 133 MB/sec
 - has burst mode allowing a single address to be followed by multiple data
 - to expand the number of available expansion slots, PCI-to-PCI bridges are used
 - multiple bridges can be cascaded, theoretically allowing unlimited numbers of PCI slots to be configured in a single system

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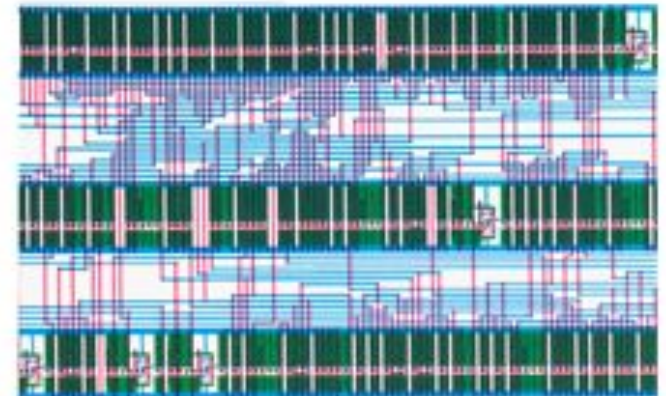
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ASIC

- An IC is customized for a particular use, rather than intended for general-purpose use
 - can't be changed after manufacturing
- Could be as small as an adder or a divider, or big as a GPU or SOC(System on a chip)
- Standard Cell Design method
 - uses tools to combined many standard cells (logic blocks) which are made already and could achieve high density and performance
 - EDA physical tools could be introduced to accelerate the back-end (RTL to Chips) process. (synthesis, placement, channel routing, timing analysis)



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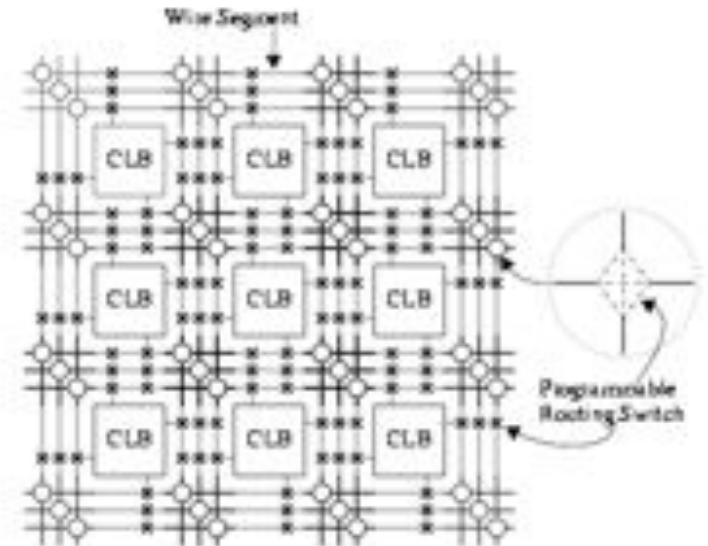
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FPGA

- An type of IC which function could be configured after manufacturing
 - is configured by HDL(Verilog,VHDL), same as used for an ASICs
 - could implement any logical function as ASIC could perform
 - has nearly no costs to reconfigure the functionality
- Constituted by configurable logic component called “Configurable Logic Blocks” and a hierarchy configurable interconnects
 - complex(Multiplier, divider,...) and simple(AND,OR,...) combination functions
 - memory blocks includes simple flip-flops or SRAM, SD-RAM
 - programmable routing switches



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	FPGA	ASIC
Speed	lower clock frequency can be achieved. (3 times slower)	
Power efficient	Less energy efficient (7 times as much dynamic power)	
Area	18 times as much area in same function	
Gate (logic) count	100 M~300M	> billions
Time to market	Easy to fix bugs No back-end effort	Back-End testing and verification
Verify	Easy to verify & test	Need time to get feedback and extra effort
Cost (mostly in design cost)	No non-recurring engineering cost No tape-out IC costs	IC costs are rising aggressively

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Intellectual Property Cores

- A reusable unit of logic, cell, or chip layout design that is the intellectual property of one party.
 - is derived from the licensing of the patent and source code copyright
 - can be used as building blocks within ASIC chip designs or FPGA logic designs
- Types of IP cores
 - soft IP cores are offered as synthesis-able HDL
 - hard IP cores are offered as low-level physical description
- Most successful example is ARM Ltd
 - does not manufacture and sell CPU devices based on its own designs, but rather, licenses the processor architecture to interested parties
 - average nearly 1,000,000 dollars per license(65 licenses in 2006), and 0.1 dollar per unit shipped(2.45 billion units in 2006)

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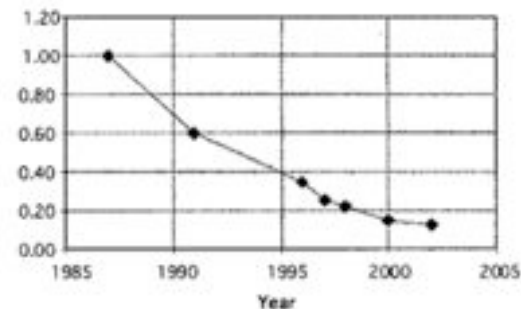
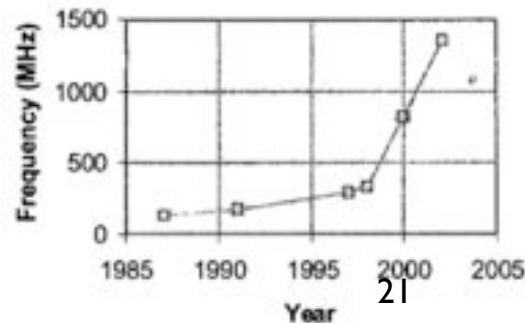
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FPGA in Avionics Computers

- Avionics computers are increasingly being implemented as soft IP cores processors within FPGAs
 - safety-critical certified hardware is extremely expensive
 - certified FPGA platforms may be shared across versions and products because it allows redesign
 - easy to be ported to the latest chip without many efforts(costs)
 - since the implementation is soft, it's allowing for design errors to be corrected and possible to implement new functionality
 - the timing(clock freq.) and the process of of FPGA is dramatically improve recently



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Issues on Avionics Computers

- Must be operated under extreme and harsh conditions
 - numerous radiation effects, extreme temperature conditions, and vacuum(low pressure)
- Remote, inaccessible, and critical nature requires special design
 - enables reliability, remote and on-line testability, self diagnostics, and fault-tolerance
- Due to extensive development and testing, radiation hardened chips tend to lag behind the cutting edge of developments
- Hard to insert new generations of technologies since given the inherent high cost and small market

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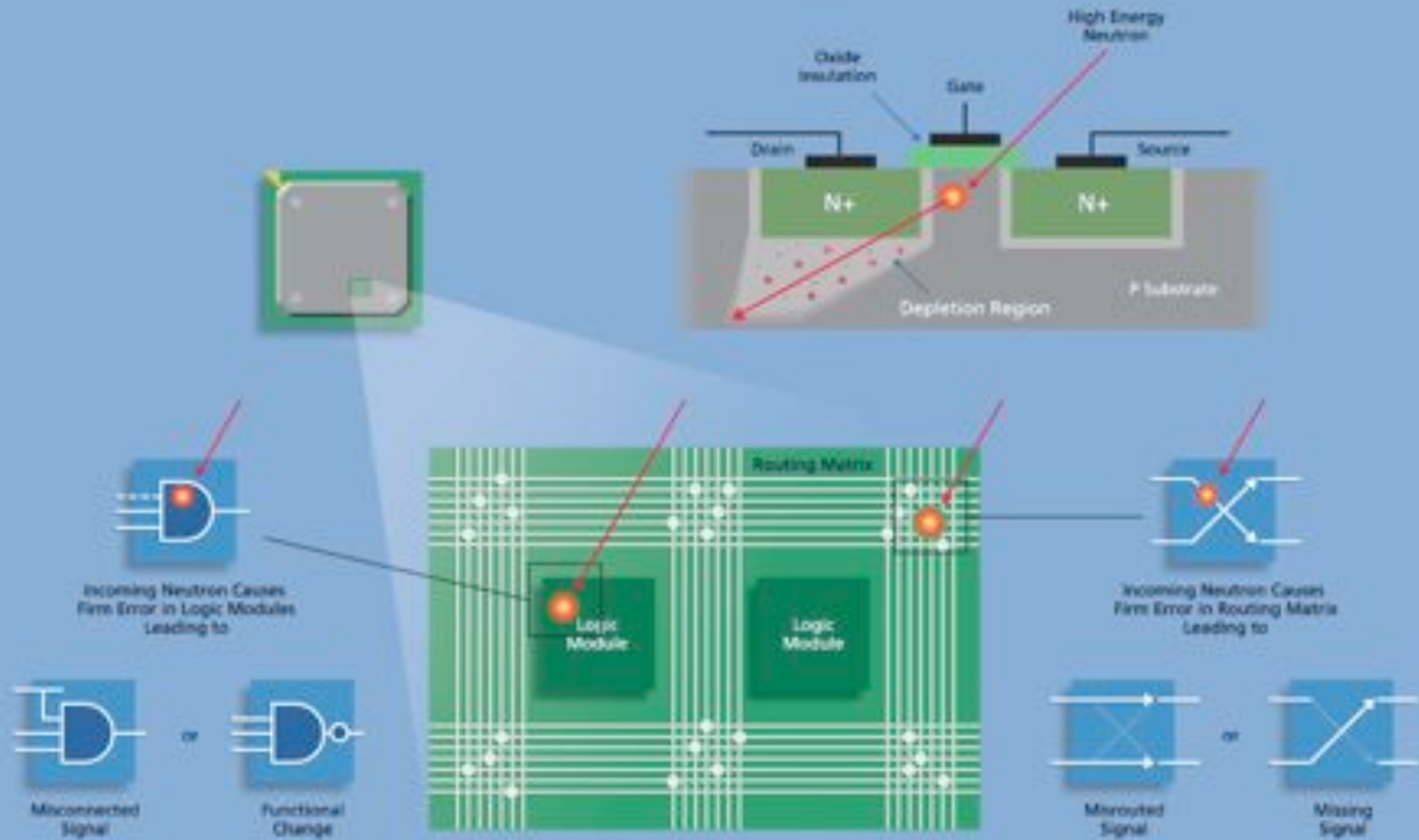
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Radiation Hardened (Rad-Hard)

- A method of designing and testing electronic components and systems to make them resistant to damage or malfunctions caused by ionizing radiation
 - major sources: cosmic rays, solar particle, or nuclear explosions
 - single charged particle can knock thousands of electrons loose, causing noise and spikes
 - a single-event effects(SEE): disturbance of an active electronic device caused by a single energetic particle
 - single-event upsets(SEU)--changes of bits caused by a single ion interacting with the chip. Don't cause lasting damage but may cause lasting problems which cannot recover. (Soft error)
 - single-event hard error(SHE)
 - causes permanent changes

Figure 1: Effects of Neutrons on SRAM FPGAs



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Rad-Hard Techniques

- Physical
 - is manufactured on Silicon On Insulator(SOI) technology
 - uses bipolar circuit
 - uses magnetoresistive RAM (MRAM)
 - shielding the package against radioactivity
- Logical
 - error correcting memory(ECC) which contains additional parity bits to check and correct corrupted data. A "scrubber" circuit must continuously sweep the RAM
 - redundant elements in system level or circuit level
 - use watchdog timer force a hard reset to the system if radiation caused to operate incorrectly

Ruggedization

- A computer specifically designed to reliably operate in harsh usage environments and conditions, such as strong vibrations, extreme temperatures and wet or dusty conditions
- Popular standards: MIL-STD-810, US Military Standard
 - a broad range of environmental conditions
 - contains environmental laboratory test methods that are applied using specific test guidelines. And, test methods are to be selected and tailored to generate the most relevant test data possible, and incorporated into a system's specification
- DO-160/Ed-14
 - is a standard for environmental test of avionics hardware by RTCA
 - outlines a set of minimal standard environmental test conditions and corresponding test procedures for airborne equipment

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Avionics Computer

- IBM AP-101, regarded as general purpose computer, used most notably in space shuttle, B-52(mid 50s), and F15(mid 70s)
 - is a radiation hardened avionics computer
 - uses TTL integrated circuit (only Bipolar and resistors)
 - shares its general architecture with IBM System360
 - 16 32-bits registers, 154 instructions, 20bits for addressing memory(1MB memory), both fixed-point and FP arithmetic(avg. 480,000 instruction/sec), 61 interrupt into 20 priority levels
 - uses five AP-101 in space shuttle (Four redundancy, one backup)



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PowerPC

- It's short for Power Optimization With Enhanced RISC- Performance Computing (PPC) and is introduced in 1992 by Apple-IBM-Motorola alliance.
- It's designed along RISC principles and allow for superscalar implementation. (CISC in Intel x86 CPUs)
 - achieved benchmark test scores that matched the fastest x86 CPUs
 - exists in both 32-bit and 64-bit implementation
 - uses Power ISA (Power Architecture)
- It became popular embedded and high-performance processors being used by Apple Macintosh lines (until 2006).
- almost all general-purpose and embedded OS.(VxWorks, LynxOS, eCos,...) support PowerPC
- Now, it focuses toward game consoles, Xbox360(Xenon);Wii(Broadway);PS3 (Cell)

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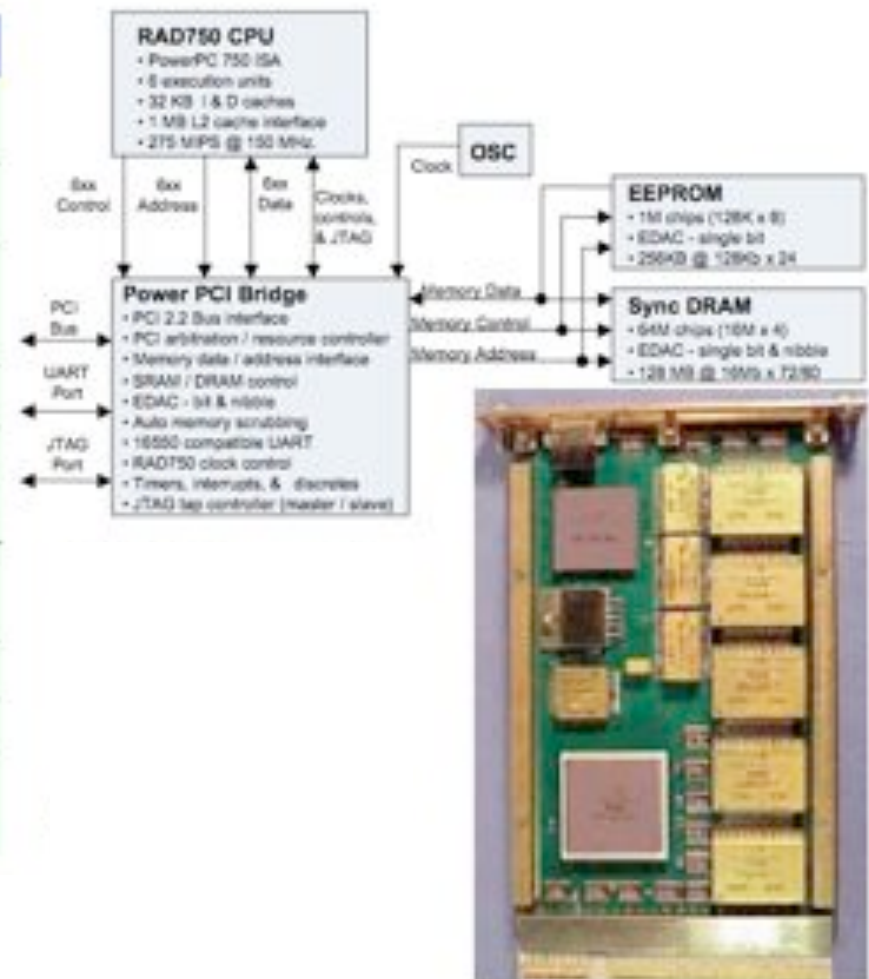
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PowerPC as an Avionics Computer

- RAD750 -- Radiation hardened single board computer for airborne application (2005) by BAE.

Specifications	
Form Factor	CompactPCI 3U (100 mm x 160 mm.) Weight: 549 grams
Processor	RAD750 240 Dhrystone 2.1 MIPS @ 133 MHz.
Radiation Hardness	Total Ionizing Dose: > 100 Krad (Si) SEU: < 1E-5 upsets/day (W.C. 90% GEO) Latchup: Immune
Performance (estimated)	5.8 SPECint95 3.5 SPECfp95 @ 133 MHz.
PCI Backplane Bus	32 bit, 33 MHz., PCI version 2.2 Peak Bandwidth: 130 MB/s write 90 MB/s read Can be keyed for System or Agent Slot
Power Supply	3.3 V + / - 10% (2.5 V generated via on-board regulator)
Power Dissipation (typ)	10 W
Roll Temperature Range	-55°C to +75°C
Mean Time Between Failures (MTBF)	Greater than 390K hours



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RAD750 CompactPCI SBC

- bases on PowerPC 750
 - 10.4M transistors, 133~200MHz (240~366 MIPS)
 - 10^{-11} upsets/bit-day radiation hardness
 - Mean Time Between Failures(MTBF) > 4.3 M hours
- With a companion ASIC called Power PCI
 - 33 MHz PCI backplane bus and 10^{-10} upsets/bit-day radiation hardness
- \$200,000 per board
- by 2010, 150 RAD750 used in a variety spacecraft.
- WindRiver VxWorks Os
 - multi-tasking kernel, dynamic load of user program

RAD750 Block Diagram

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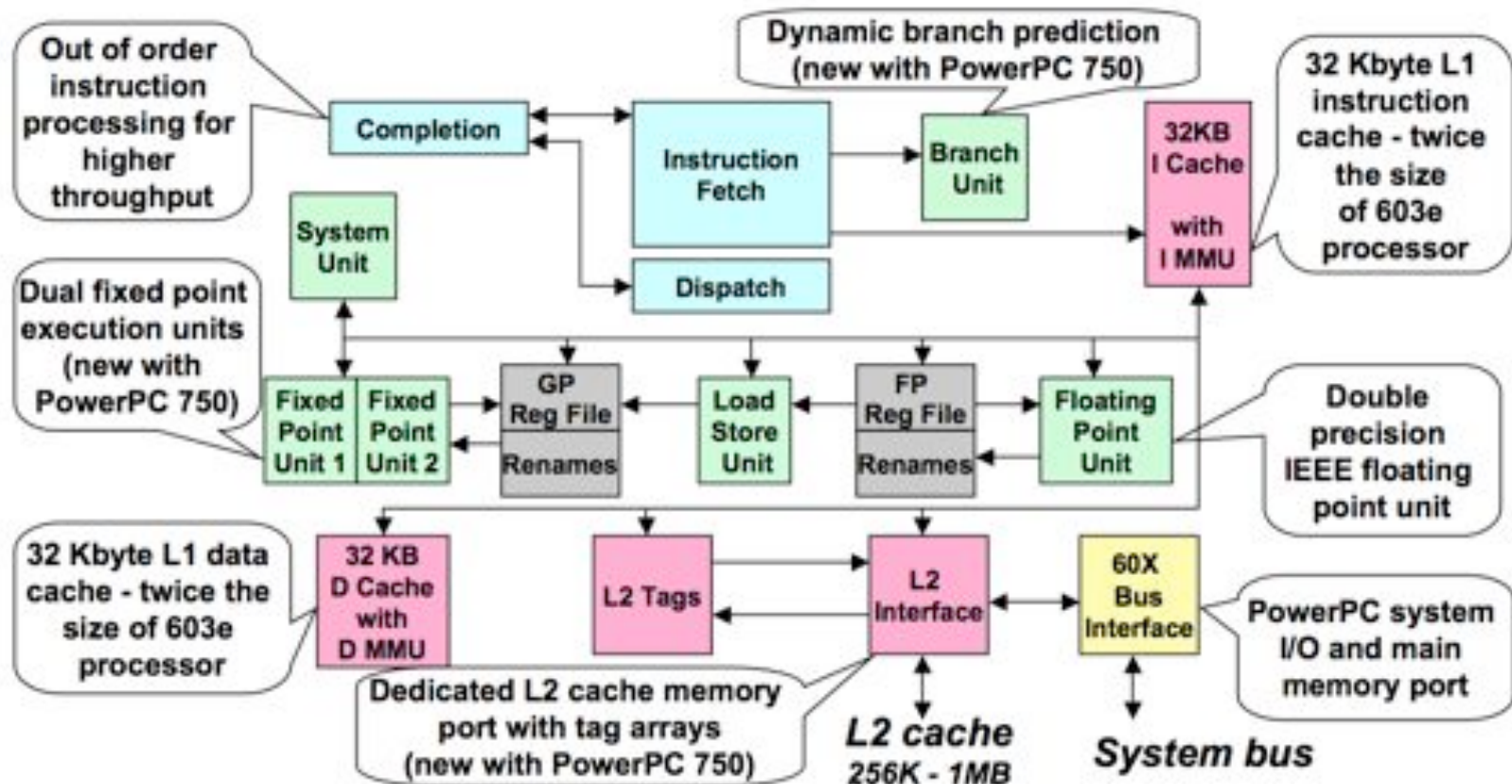
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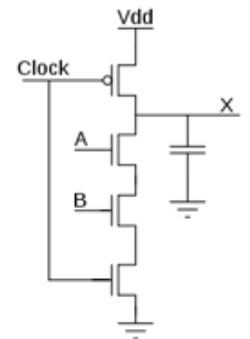
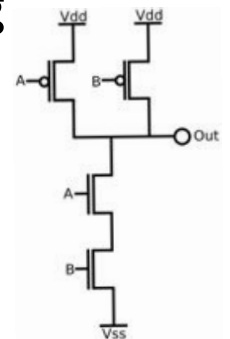
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RAD 750 Features

- Inherent PowerPc 750 power management features
 - “Doze”: keeps the snooping function and cache active
 - “Nap”: disables snooping but maintain PLL
 - “Sleep”: shuts PLL and need approximately 100ms returning time
- Uses Static circuit instead of dynamic circuit
 - noise-tolerance is better but slower
- Uses SEU hardened but bigger-sized RAM cell



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Freescale's e600 SOC

- It's built on Power Architecture, and leveraging 90 nanometer silicon-on-insulator (SOI) technology
 - endures harsh elements in space (Radiation-hardened). And , it is immune to upset and latch up(SEU and SEL)
- Applications today require more and more processing power within existing system
 - the speed ranging over 1.33~1.7GHz(PowerPC G4) and has dual core version, 1.5 GHZ and 2.3 MIPS/MHz
- Use ECC-protected Cache

Freescal's e600 SoC

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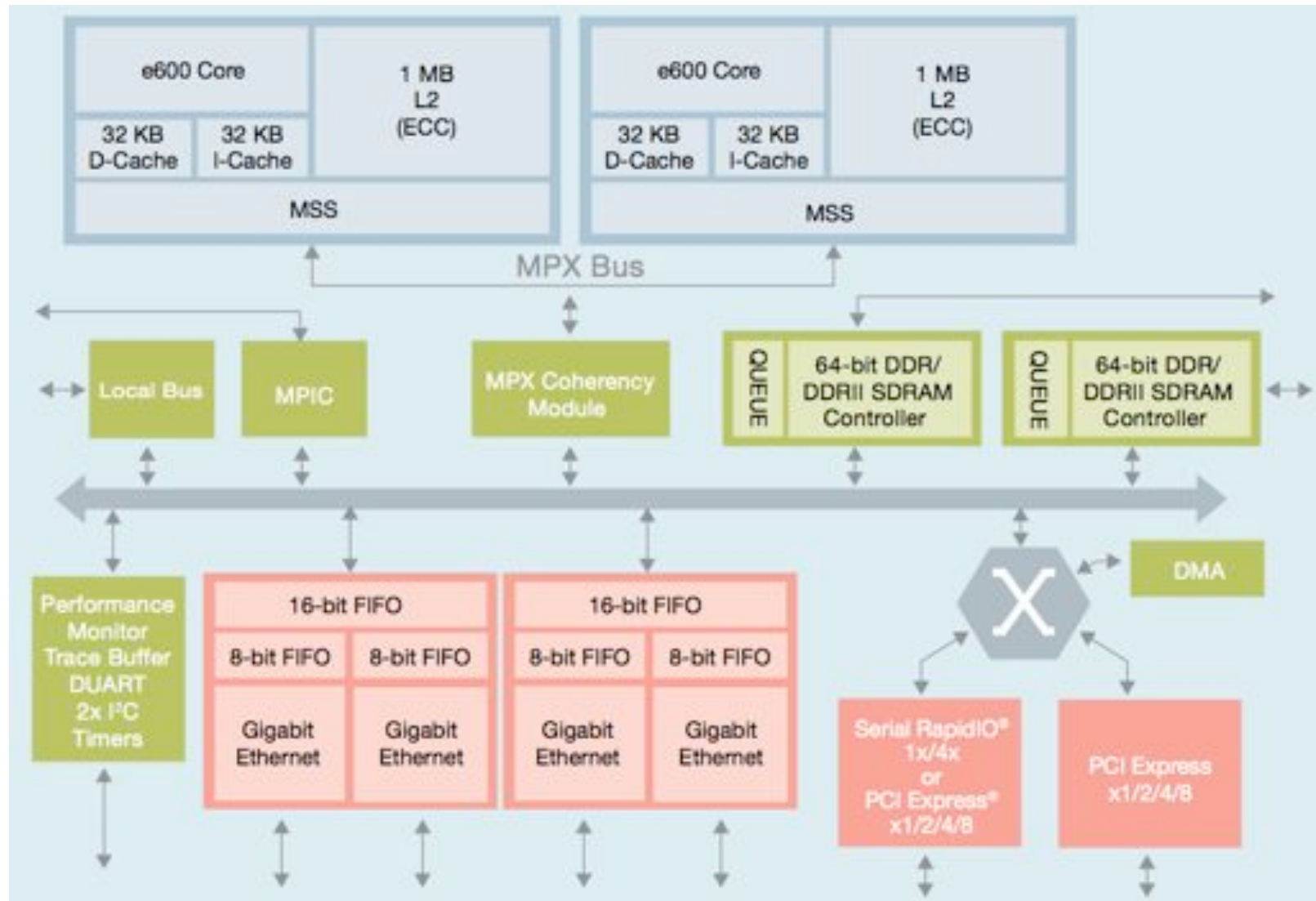
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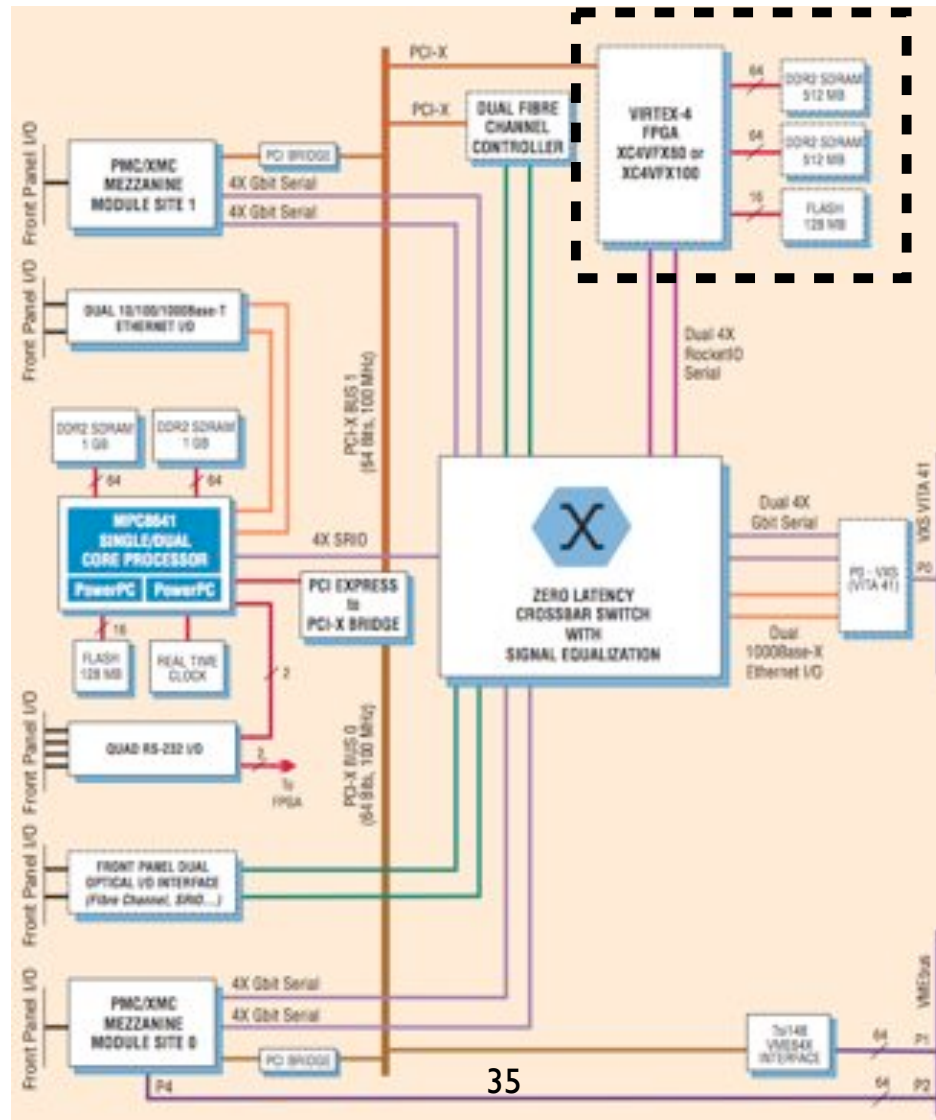
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e600 with FPGA SBC

- Support for VxWorks 653 RTOS (on Boeing 787 Dreamliner) and Linux.



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GE's V7788 SBC(intel)

- It's single board with Intel Core 2 Duo 2.16 GHz and up to 2 Gbyte DDR2 SDRAM.
 - contains 4 Mbyte L2 cache
- This board integrates the Intel 945GME Express Chipset and offers a very rich I/O set
- I/O options include dual Gigabit Ethernet, two SATA interfaces, four USB 2.0 ports, keyboard/mouse/SVGA on the front panel, as well as a PCI-X capable PMC site
- Operating System Support for Windows XP, VxWorks 653 RTOS (on Boeing 787 Dreamliner), and Linux

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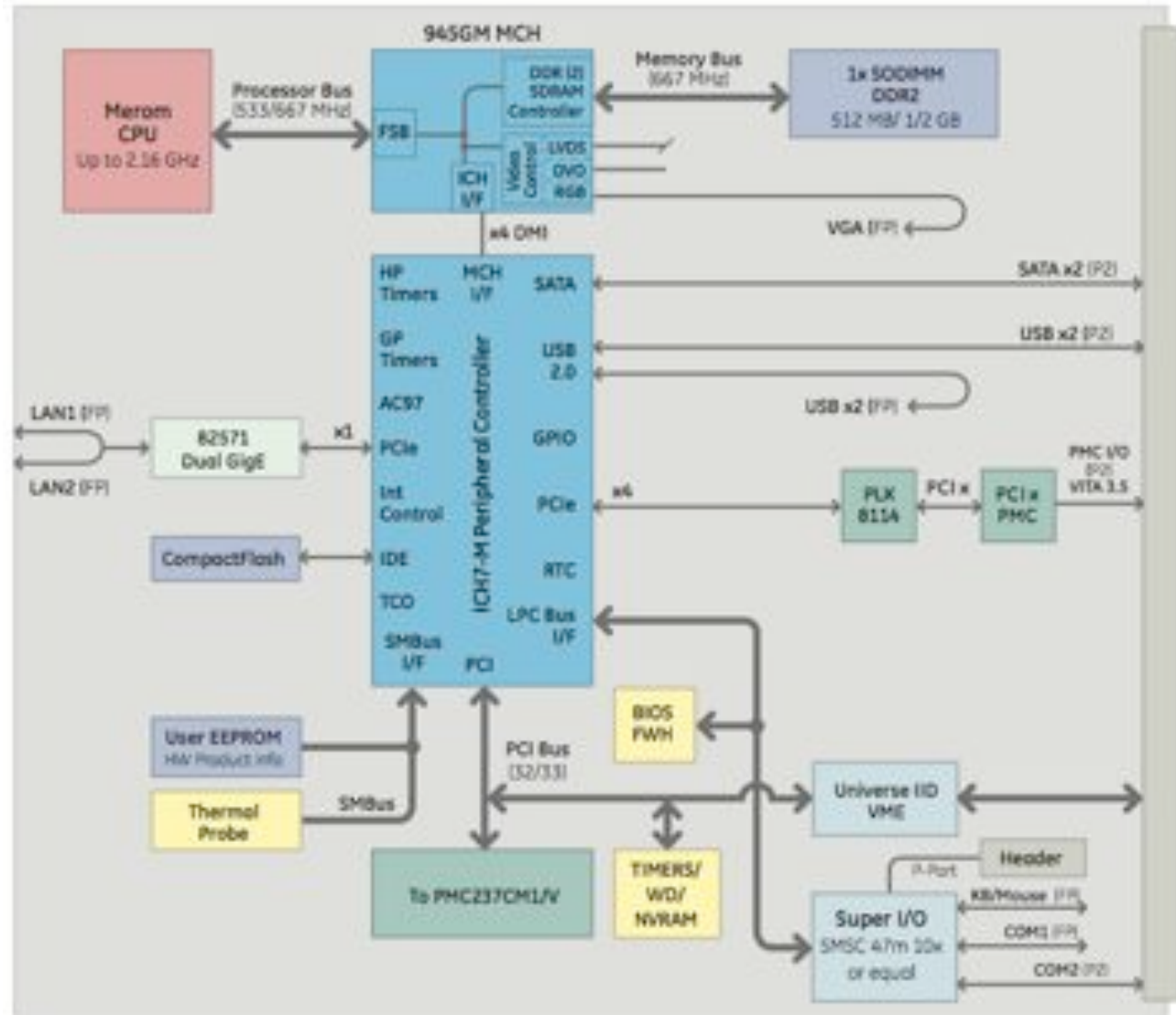
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GE's V7788 SBC(intel)



Energy Issues

- The power in a CMOS circuit consists of static and dynamic power
 - Static power
 - depend on the supply voltage
 - Dynamic power
 - $P = \sum \alpha f C V^2 (\propto V^3)$
 - α : Switching activity for the node
 - f : Clock frequency
 - C : Capacitance of the node
 - V : Supply voltage

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HW Design for Low Power

- Lowering the supply voltage
 - the problem is that it slows the timing performance of the chip
 - use parallelism to compensate the performance
 - standard voltage in I/O modules; low voltage in core modules
- Reducing capacitance and switching activity
 - low-power standard cell library (low-power process)
- Sizing and other synthesis techniques
 - gate sizing can produce a significant power savings in many designs. And, synthesis tools can do this automatically, without any requirement for changing the HDL code

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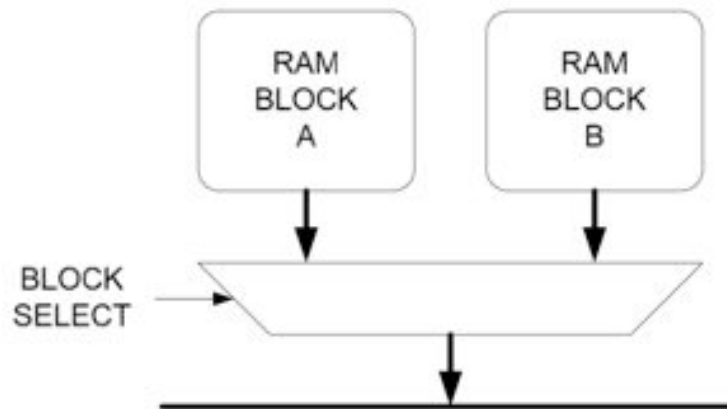
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HW Design for Low Power

- Memory architecture
 - use EDA tools to trade-off between area, power, and speed
 - instead of using a single, deep memory, it may be possible to partition the memory into several blocks, selected by a decode of the upper or lower address bits. Only the block being accessed is powered up



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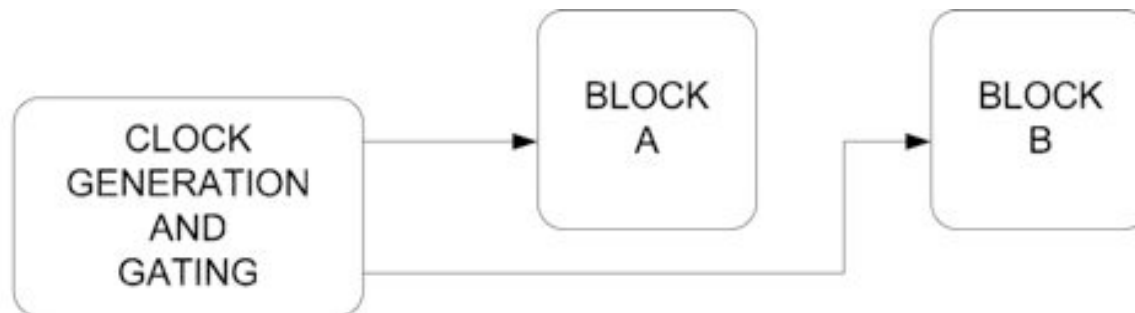
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HW Design for Low Power

- Clock Distribution
 - a significant portion of the overall power is in the clock.
 - uses clock gating: (Shutting down clock distribution to part of the circuit which is not running)
 - the clock gating circuit itself tends to be technology dependent and not reusable
 - isolates the clock gating in a separate clock generation block allow Block A and Block B to be completely usable



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HW Design for Low Power

- Improvement results [Low Power Digital CMOS Design, 1995]
 - 21x reduction in power by lowering the voltage from 3v to 1.1v
 - 3–4x reduction from gate sizing, low-power I/O cells, and similar gate-level optimization
 - 2–3x improvement by clock gating
 - 8x improvement in a memory array by using the multi-block technique

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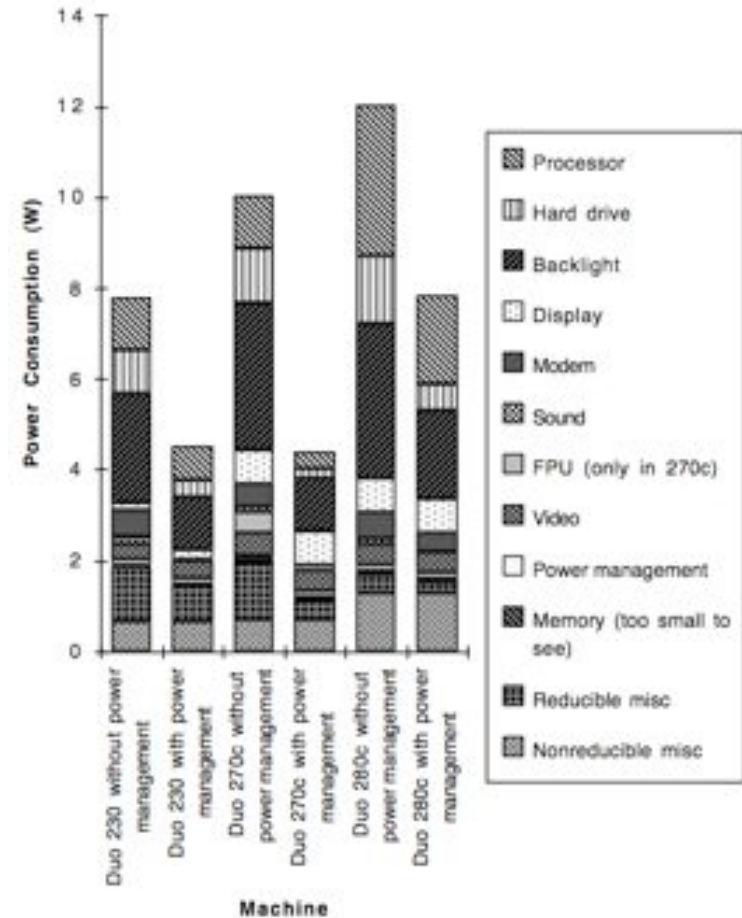
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System-Level Power Issue

- Knowing how much a technique reduces the power consumption of a component is not sufficient
- the reduction on the component depends on the fraction of total system power due to the component
- 10%~30% consumption on CPUs
- 12% on hard drive
- 30% on Backlight



J. Lorch, "A Complete Picture of the Energy Consumption of a Portable Computer", 1995

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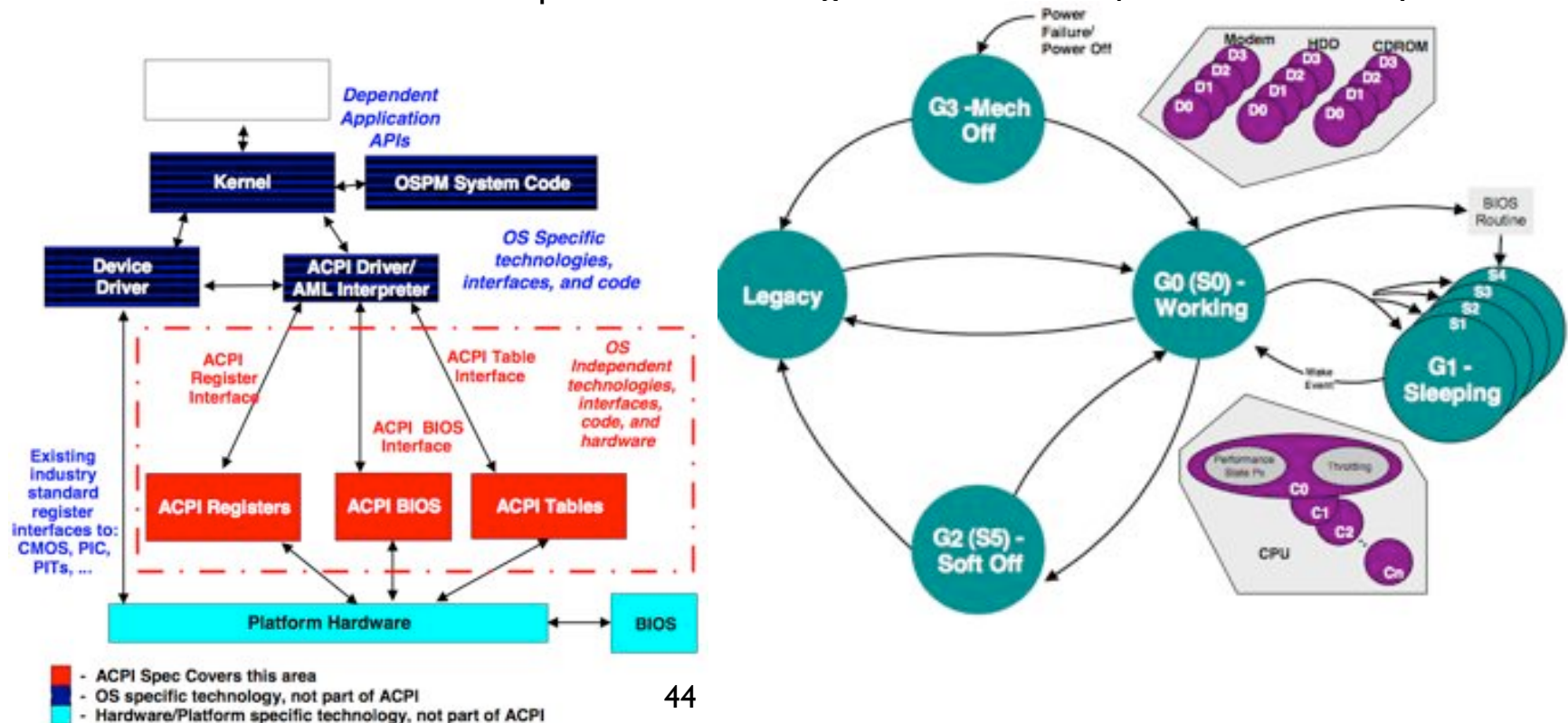
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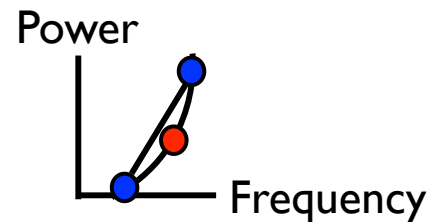
System-Level Power Issue

- Optimizing the system for maximum power efficiency is done as a combination of SW(OS) and HW
- most OS use “ACPI” standard for optimizing the system power consumption
- ACPI is an “interface” specification allowing OSPM to control power state directly



CPU Power State

- Power-state(P_x): predefines different supply voltage
- According to the pervious researches, it shows that static setup is better than dynamic setup since the power distribution ($P \propto F^3$) is convex



P-State	Frequency	Voltage	Power
P0	1.6 GHz	1.484 V	25 Watts
P1	1.4 GHz	1.420 V	~17 Watts
P2	1.2 GHz	1.276 V	~13 Watts
P3	1.0 GHz	1.164 V	~10 Watts
P4	800 MHz	1.036 V	~8 Watts
P5	600 MHz	0.956 V	6 Watts

P-State Operating Points and Power Consumption for the Intel Pentium M 1.6 GHz CPU

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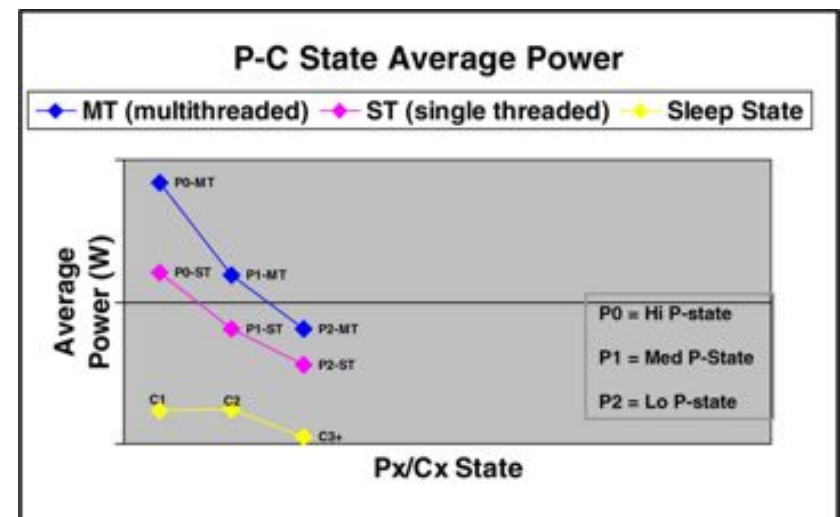
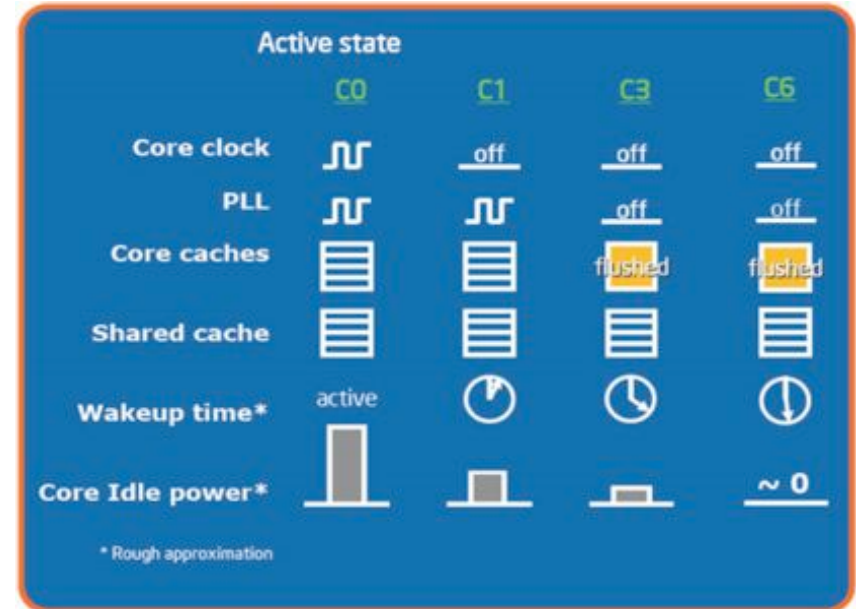
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CPU Freq. in Linux

- There are five in-kernel governors available for use with the CPUfreq subsystem.
 - Performance governor: Always highest frequency (can adjust the available max. frequencies)
 - Powersave governor: Always lowest frequency (can adjust the available min. frequencies)
 - Userspace governor: Manual frequencies (set specific frequency by user)
 - Ondemand governor: Frequency change based on processor utilization
 - if the utilization exceeds up_threshold, set the frequency to the highest available. If below up_threshold, it set to the next low frequency. (can adjust the available range of frequencies and up_threshold and sampling rate)
 - Conservative governor: A more gradual ondemand governor
 - if the utilization exceeds up_threshold, set the frequency to the next high frequency. If below the down_threshold, it set to the next low frequency. (can adjust the available range of frequencies and thresholds and sampling rate)

CPU Idle State

- Idle State of CPUs (C-state):
 - newest CPUs provide various idle state with different power consumption
 - the lowermost state could decrease CPUs' power consumption nearly to zero
 - tradeoff:
 - a deeper idle state consumes lower energy at the expense of higher exit latency



CPU Idle State

- Package C-state: A package state is an idle state in which all cores in a package reside (the package size is four in Core i7)
- During package idle states, shared resources—L2 cache, PLL, clock tree, and voltage plane—are shut down for saving more energy
- the package states can only be triggered when all cores in the package are in same idle state

Core_0 State

Core_0	CC0	CC1	CC2	CC3	CC4
Core_1	CC0	CC1	CC2	CC3	CC4
CC0	C0	C0	C0	C0	C0
CC1	C0	C1	C1	C1	C1
CC2	C0	C1	C2	C2	C2
CC3	C0	C1	C2	C3	C3
CC4	C0	C1	C2	C3	C4

Core_1 State

CPU Idle in Linux

- Ladder
 - takes a step-wise approach to selecting an idle state
- Menu
 - looks at different parameters like the expected sleep time, latency requirements, etc., and then picks the deepest possible state
 - aims at getting maximum possible power advantage with little impact on performance

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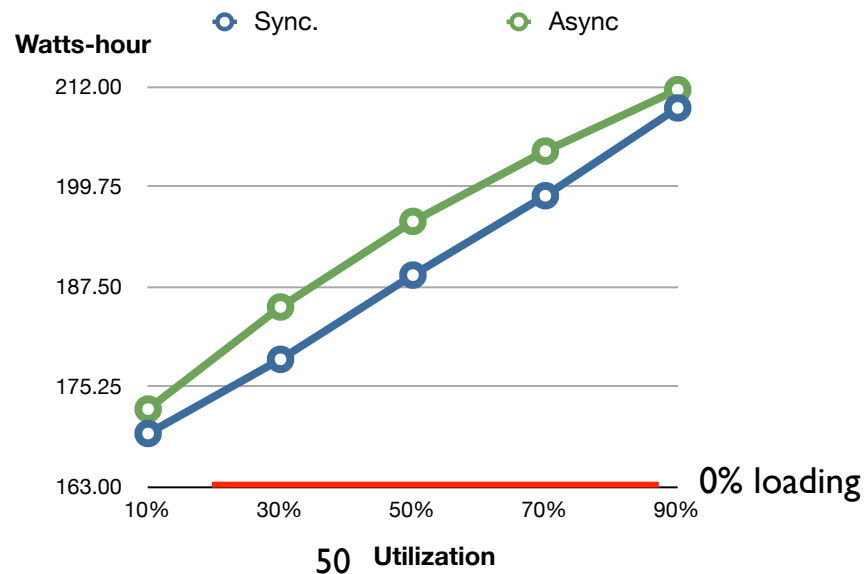
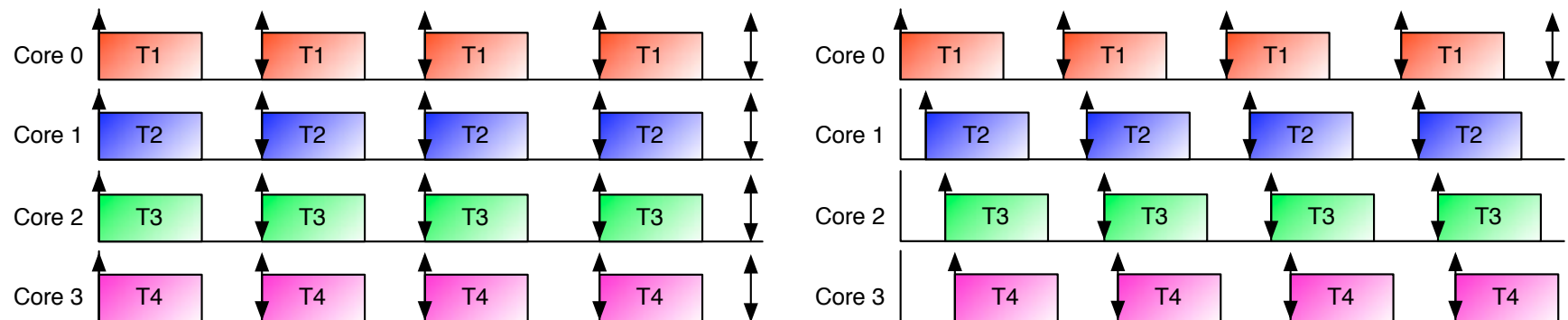
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Package state vs Core state

- Setup different (a)sync. released task sets with various utilization rates with constant periods(100ms)



Certification

- While DO-178 is prevalent as a desired and acceptable measure of avionics software quality and safety, DO-254 covers all aspects of the avionics hardware design and deployment
- RTCA DO-254 (EUROCAE ED-80): Design Assurance Guidance for Airborne Electronics Hardware
 - is released in 2000 but formally recognized in 2005 by FAA
 - provides a basis for the certification of in-flight complex electronics hardware devices. Complex electronic hardware includes devices implemented in FPGAs and ASICs
 - shares a common heritage and structure with DO-178
 - five design assurance levels, A-E.(same notion in DO-178)

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RTCA DO-254

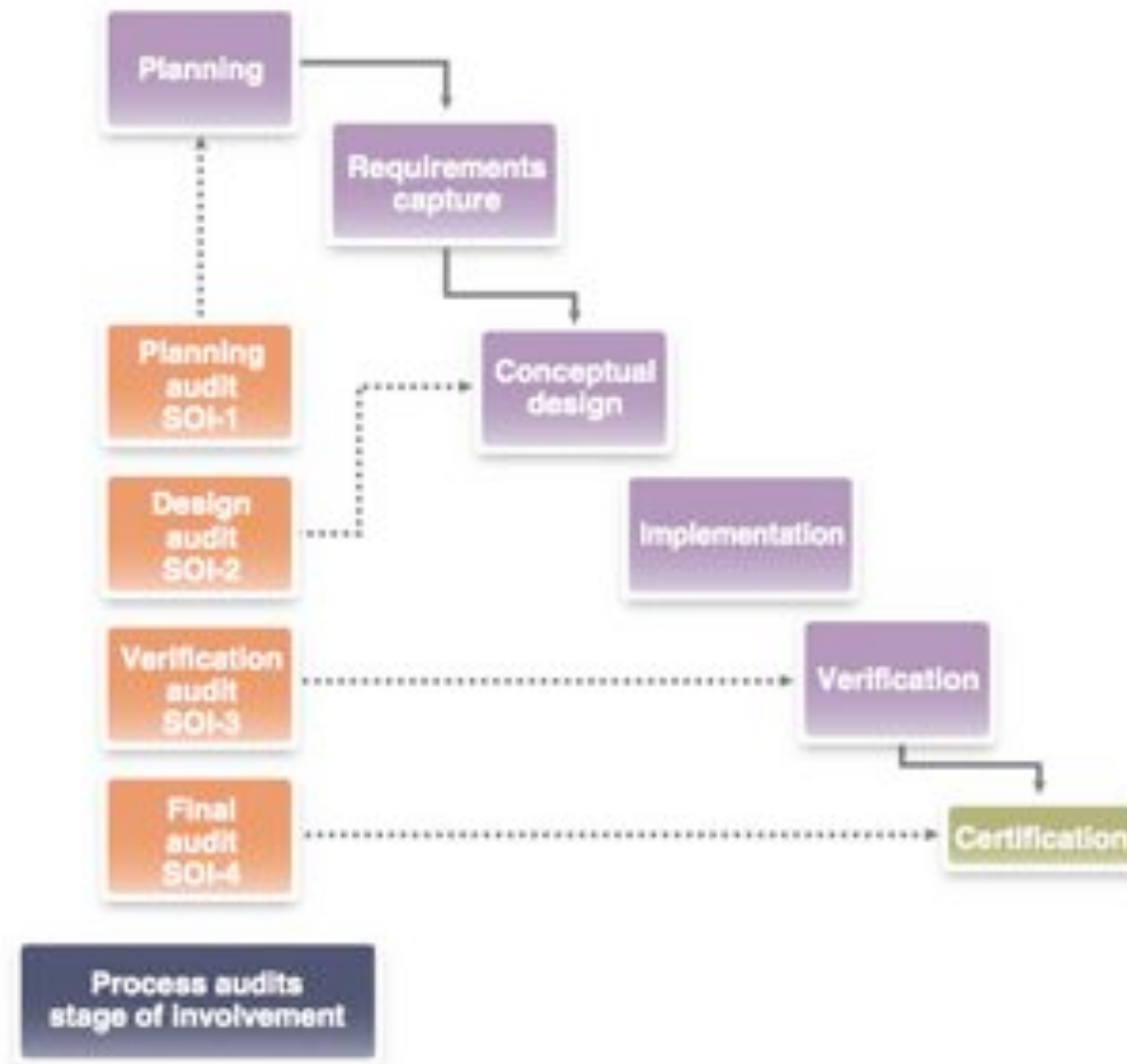
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- Mandates clearly specified and validated requirements
- Requires Accurate implementation of those requirements
- Requires thorough verification to prove the design meets those requirements
- Requires traceability of the requirements to their implementation
- Provides only guidance for achieving each level, but it doesn't specify how to implement the standard
- the task is left for the manufacture, and the special process is approved by *Designated Engineering Representative (DER)*, who examines the design and verification processes



DO-254 Process Flow

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Requirements Capture and Traceability



- Documents the life of a requirement and provides bi-directional traceability between various associated requirements
 - enables users to find the origin of each requirement and track every change which was made to this requirement
 - often uses commercial requirements capture and tracking tools such as DOORS
 - employ data “tags” derived from the original requirements document, and these tags are placed in VHDL, test-bench and implementation file
- From these captured requirements, two documents are derived: a design specification, and a verification plan
- Also produces PHAC(Plan for Hardware Aspects of Certification)
 - refers to the verification plan and describe the methodology used to achieve total verification
 - specifies the EDA tools to be used in the project, and outline the method of tool assessment for each
- All the configuration using in design(All codes and tool setup) and verification process

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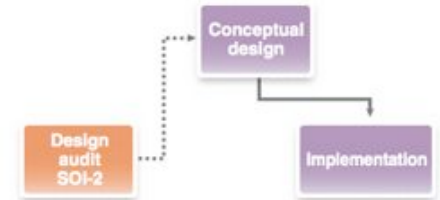
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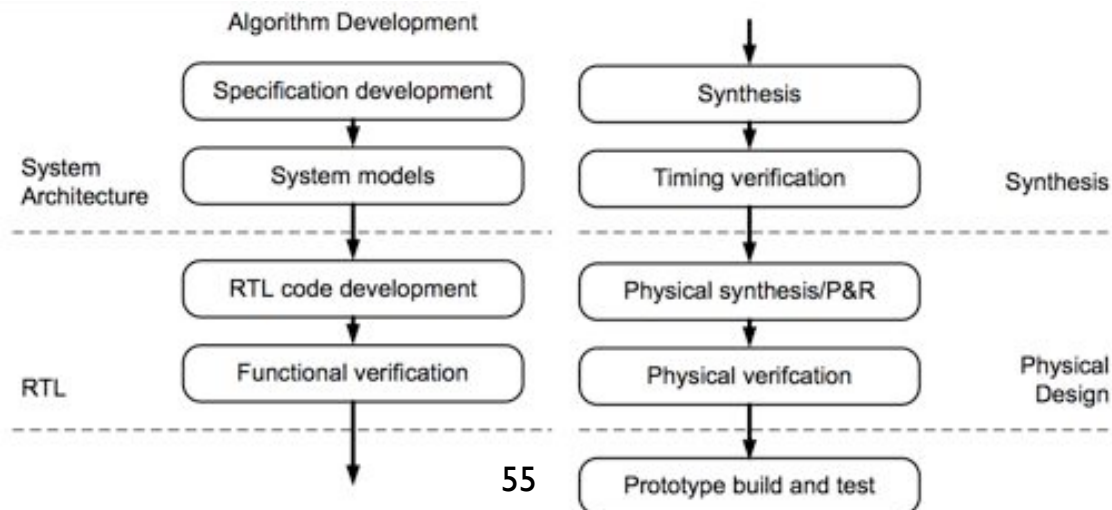
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DO-254 Compliant Implementation



- Designers will start with a concept, and develop RTL code, using assertions along the way to check the functionality vs. the set requirements
- The output of the synthesis tools must also be verified
- gate-level netlist is equivalent to the RTL implementation. For smaller designs, gate-level simulation may be sufficient; larger, more complex designs require a more complete approach-equivalence checking(logical model checking)



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Verification in a DO-254 Flow

Verification
Audit
SOI-3

Verification

- Verification is the most crucial phase since this is where the design is checked vs. the initial formal requirements.
- Test bench design
 - all response checking should be done automatically
- Code coverage is necessary for certification to levels A and B.
 - should spell out goals for code coverage (at minimum, 100% statement coverage is required by DO-254)

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Verification Methodology

- Directed testing methodology: executing through simulation one test per requirement
 - disadvantage: It is often necessary to add new tests to address untested code and corner cases. The bulk of modern electronic designs are sufficiently complex that complete verification of all functional corners using a directed test approach is impractical
- Constrained random verification:
 - requires the implementation of a sophisticated, self-checking verification environment which can predict and verify the behavior under all conditions
 - there is not a one-to-one correspondence between the formal requirements and the associated tests
 - must run many test with different random seeds, and gather these result in coverage information until 100% coverage is achieved

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DO-254 Certification

Final
Audit
SOI-4

Certification

- The Hardware Accomplishments Summary (HAS) is a document which assembles the compliance and completion data accumulated during the project.
- Review of the HAS is part of the final audit by the manufacturer (DER).
- after that, they can submit the appropriate paperwork to the FAA for certification.

