

2 December

- 1 class to go
- CCR
- Exam Review



12/2/2004

Comp 120 Fall 2004

1

1

- 1 A branch instruction changes the flow of control by
- a) changing SP (stack pointer)
 - b) changing the PC (program counter)
 - c) changing an address register
 - d) none of the above.

12/2/2004

Comp 120 Fall 2004

2

2

In a machine with 32 registers and instructions that need 3 registers (like MIPS). How many bits of the instruction are required to specify the registers?

- a) 32 bits
- b) 3 bits
- c) 18 bits
- d) 15 bits

12/2/2004

Comp 120 Fall 2004

3

3

- Which of the following **cannot** be EXACTLY represented by an IEEE single-precision floating-point number?
 - a) 0
 - b) 10.2
 - c) 10.25
 - d) 10.5

12/2/2004

Comp 120 Fall 2004

4

4

All of the following equations are true for the idealized numbers you studied in algebra. Mark the ones that are true for IEEE floating point numbers. Assume that all of the numbers are well within the range of largest and smallest possible numbers (that is, underflow and overflow are not a problem)

- a) $A+B=A$ if and only if $B=0$
- b) $(A+B)+C = A+(B+C)$
- c) $A+B = B+A$
- d) $A*(B+C) = A*B + A*C$

12/2/2004

Comp 120 Fall 2004

5

5

- Place the following elements of the memory hierarchy in order of increasing access time by numbering them sequentially starting with 1 for the least access time.
 - a) L1 Cache
 - b) Register file
 - c) Network
 - d) Main Memory
 - e) L2 Cache
 - f) Disk

12/2/2004

Comp 120 Fall 2004

6

6

1. Fill in the following truth table.

A	B	C	A or B	(A and B) or (A and C)	(A+B+C) is odd	(A+B+C)>1
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

12/2/2004

Comp 120 Fall 2004

7

7

- Using 2's complement arithmetic, negate 0x1234ffff. What is its value in hex?
 - 0xedcb0000
 - 0x1234ffff
 - 0xffff4321
 - 0xedcb0001

12/2/2004

Comp 120 Fall 2004

8

8

- Consider the address 0x00429234. Which cache line of a 32k byte direct-mapped cache will this address access if the cache line size is 16 bytes?
 - 0x00000234
 - 0x00042923
 - 0x00000123
 - 0x00000429

12/2/2004

Comp 120 Fall 2004

9

9

- For the same address as in question 10 (0x00429234), assuming a virtual-memory page size of 4096 bytes, what is the virtual page number?
 - 0x00429234
 - 0x00000429
 - 0x00000000
 - 0x00000042

12/2/2004

Comp 120 Fall 2004

10

10

- A processor with cycle time = 2 nanoseconds and CPI=1 when there are no misses has a cache-hit rate of 90% and a cache-miss penalty of 100 nanoseconds. What is the effective CPI including the misses?
 - 1.5
 - 6
 - 51
 - 4.5

12/2/2004

Comp 120 Fall 2004

11

11

- Suppose we decrease the cycle time in above processor to 1 nanosecond with the same cache and memory system. What is the effective CPI for this system including misses?
 - 1.6
 - 101
 - 11
 - 90

12/2/2004

Comp 120 Fall 2004

12

12

- Order the following computer configurations by decreasing performance/price ratio. That is, put number 1 by the system that gives the most performance for the dollar, 2 by the system with next best, and 3 by the system with the worst price/performance.
 - a) The system of question 12 @ \$100.
 - b) The system of question 13 @ \$125.
 - c) The system of question 12 but with a bigger cache and hit rate = 95% @ \$150.

12/2/2004

Comp 120 Fall 2004

13

13

- Machine A has CPI=1.5. Machine B has CPI=1.6. Is Machine A necessarily faster than B?
 - a) Yes, with the same clock rate
 - b) No.
 - c) Yes, with the same number of instructions.
 - d) Yes.

12/2/2004

Comp 120 Fall 2004

14

14

- What decimal number does this eight-bit two's complement number represent: 10110001_{two} ?
 - a) 79
 - b) 177
 - c) -79
 - d) -177

12/2/2004

Comp 120 Fall 2004

15

15

- How will the hit rate of a cache change if we double the processor clock rate?
 - a) The hit rate will go down.
 - b) The hit rate will stay the same.
 - c) The hit rate will go up.

12/2/2004

Comp 120 Fall 2004

16

16

- If all cache misses are classified as compulsory, capacity, or conflict which misses are likely to be reduced if the program is rewritten to require less memory?
 - a) Compulsory
 - b) Capacity
 - c) Conflict
 - d) Compulsory and Capacity
 - e) Compulsory and Conflict
 - f) Capacity and Conflict

12/2/2004

Comp 120 Fall 2004

17

17

- What is the total size of the page table assuming all the pages are in use, byte addressing, 32-bit virtual address, 4096-byte page size, 4 bits per page for flags, and 32 bit physical addresses.
 - a) 3 megabytes.
 - b) 6 megabytes.
 - c) 16 kilobytes.
 - d) 4 gigabytes

12/2/2004

Comp 120 Fall 2004

18

18

- The function of the TLB is to
 - a) speed up memory access by storing data values from memory
 - b) speed up address translation by storing virtual to physical address translations
 - c) speed up the processor by storing previously computed register values
 - d) speed up character operations by storing translations of character strings to numbers

12/2/2004

Comp 120 Fall 2004

19

19

- When you try to access a virtual-memory location that is paged out, the OS is likely to:
 - a) Stall the processor until the page is loaded by hardware.
 - b) Start the disk read to get the page into memory and allow other programs to run
 - c) Terminate the program with an error message.
 - d) Start the program over with more memory allocated to it.

12/2/2004

Comp 120 Fall 2004

20

20

- How does pipelining improve processor performance?
 - a) By decreasing the clock rate
 - b) By decreasing the number of cycles required to complete an individual instruction
 - c) By allowing different stages of multiple instructions to execute in parallel
 - d) By increasing CPI.

12/2/2004

Comp 120 Fall 2004

21

Classes to go

0

12/2/2004

Comp 120 Fall 2004

22