Implications of Computer Organization

Lecture 16
March 9th 2023 | COMP 211-002 | Joshua Bakita
Welcome!

Today:
➔ More on the software implications of physical computer structure

Logistics:
➔ Assignment 4 part 1 posted. Part 2 coming in the next week.

Fun fact…

From normal mode, you can type `dd` to delete the current line in vim
Getting Data Before It's Needed

Beyond light speed, with caches and prefetching
Polysilicon layer of a Core Complex (CCX) Die of an AMD EPYC 7702 ES. Die size 10.32 mm × 7.34 mm.

Author: Fritzchens Fritz

Majority of the die is the L3 cache
Much of the core is the Level-2 and Level-1 cache.
Getting Data Before It's Needed

Core Complex (CCX)

L3 is 16-way
L2 is 8-way
L1 is 8-way
64B line size
32B inter-level link width

Throughput: (approx.)
Core to L1I:
- Load 32B/cycle
Core to L1D:
- Load 2x 32B/cycle
- Store 1x 32B/cycle
L1 to L2: 32B/cycle
L2 to L3: 32B/cycle

The displayed size of each cache block is directly proportional to its actual memory size

The displayed distance between the cores and each cache block is directly proportional to their access latency
Getting Data Before It's Needed

Locality

*Temporal Locality*: Recently referenced items are likely to be referenced again in the near future.

**Implications:**
➔ Best to keep most-recently-used data around, as it's likely to be used again soon

*Spatial Locality*: Items with nearby addresses tend to be referenced close together in time.

**Implications:**
➔ When fetching data, best fetch nearby data too
Questions?

Have a great spring break!

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