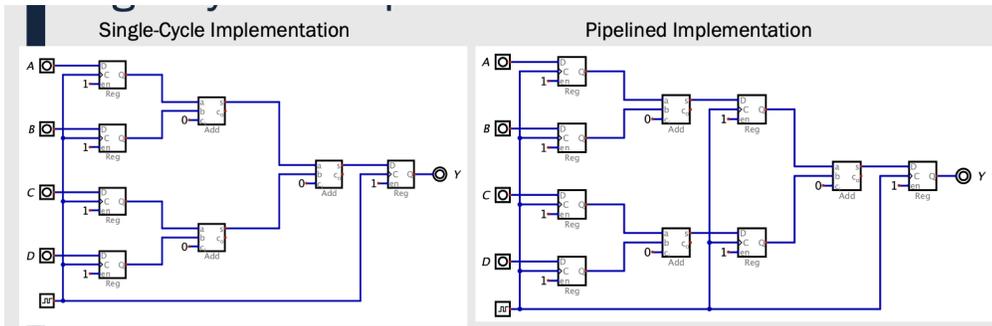


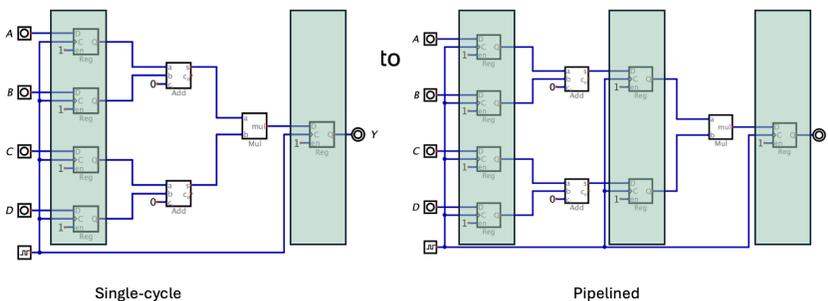
Question 1: Performance Analysis Given the single cycle and pipelined implementation of the same circuit below, answer the following questions.



- 1.1. What is the latency of an operation in the single-cycle implementation?
- 1.2. What is the latency of an operation in the the pipelined implementation?
- 1.3. Is the throughput higher in the single cycle example or the pipelined example?
- 1.4. What is the speedup for executing 10 operations?
- 1.5. If we had performed 20 operations, would the speedup be higher? Note, you shouldn't have to do any math for this

Question 2: More Performance Analysis Given the single cycle and pipelined implementation of the same circuit below, answer the following questions. Assume Clock-to-q delay = 20ps, Adder propagation delay = 480ps, and Multiplier propagation delay = 1200ps.

$$Y = (A + B)(C + D)$$



Column 1: Single Cycle Implementation

- 2.1. What is the longest combinational path?
- 2.2. What is the min clock period (critical path)?
- 2.3. If the clock period is at least the min period, how many clock cycles does it take to perform one operation?
- 2.4. If we run this circuit at the minimum clock period, how long will it take to complete 10 operations?

Column 2: Pipelined Implementation

- 2.5. What is the longest combinational path?
- 2.6. What is the min clock period (critical path)?
- 2.7. If the clock period is at least the min period, how many clock cycles does it take to perform one operation?
- 2.8. If we run this circuit at the minimum clock period, how long will it take to complete 10 operations?