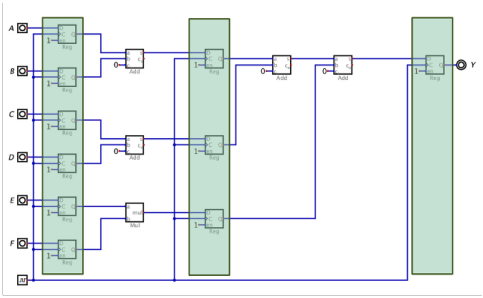
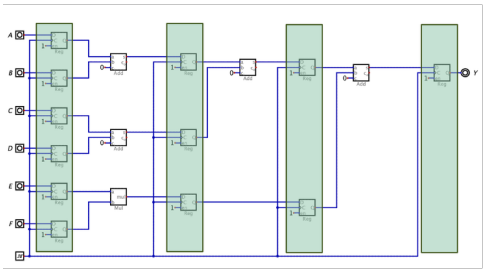
COMP311 In Class Practice 10-28-25 Name: _____

Question 1: Pipelining and Performance Analysis Below are the 2 and 3 stage pipeline diagrams for the example `Y = A + B + C + D + EF`. We are assuming a clk-to-q delay of 20ps, an adder propagation delay of 480ps, and a multiplier propagation delay of 1200ps.
The clock period is 1220ps.





Answer the following for each circuit.

2 Stages

1.1. What is the longest combinational path?

1.2. What is the min clock period? (Critical path)?

1.3. If the clock period is at least the min period, how many clock cyclde does it take to perform one operation?

1.4. If we run this circuit at the minimum clock period, how long will it take to complete 10 operations?

3 Stages

1.5. What is the longest combinational path?

1.6. What is the min clock period? (Critical path)?

1.7. If the clock period is at least the min period, how many clock cyclde does it take to perform one operation?

1.8. If we run this circuit at the minimum clock period, how long will it take to complete 10 operations?

Question 2: Performance Metrics Some additional questions given the same circuits...

2.1. What is the latency of an operation in the 2-stage pipeline?

2.2. What is the latency of an operation in the 3-stage pipeline?

2.3. Is the throughput higher in the 2-stage or 3-stage pipeline?

2.4. What is the speedup of completing 10 operations on the 2-stage pipeline vs 2-stage pipeline?