

**Question 1: Pipeline Stalls** Considering the 5-stage RISC-V pipeline discussed in lecture, would we need to add any stalls for this program?

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1 add x5, x3, x4
2 or x8, x9, x10
3 xor x14, x15, x16
4 sub x7, x5, x2
    
```

**Question 2: Pipeline Diagram with Stalls** Answer the following questions considering the 5-stage RISC-V pipeline discussed in class.

2.1. Fill out the pipeline diagram for the set of instructions.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
add x3, x2, x2															
or x4, x2, x5															
and x9, x4, x10															
sub x11, x4, x14															
add x11, x15, x18															

2.2. What is the CPI?

2.3. What is the speedup compared to a single-cycle datapath?  
 Assume pipelined clock period = 220ps and single-cycle clock period = 820ps

**Question 3: Pipeline Diagram with Stalls #2** Answer the following questions considering the 5-stage RISC-V pipeline discussed in class.

3.1. Fill out the pipeline diagram for the set of instructions.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
add x4, x3, x2															
sub x5, x6, x7															
or x8, x4, x9															
and x10, x5, x11															
sub x10, x5, x12															

3.2. What is the CPI?

3.3. What is the speedup compared to a single-cycle datapath?

Assume pipelined clock period = 220ps and single-cycle clock period = 820ps