

COMP311: *COMPUTER ORGANIZATION!*

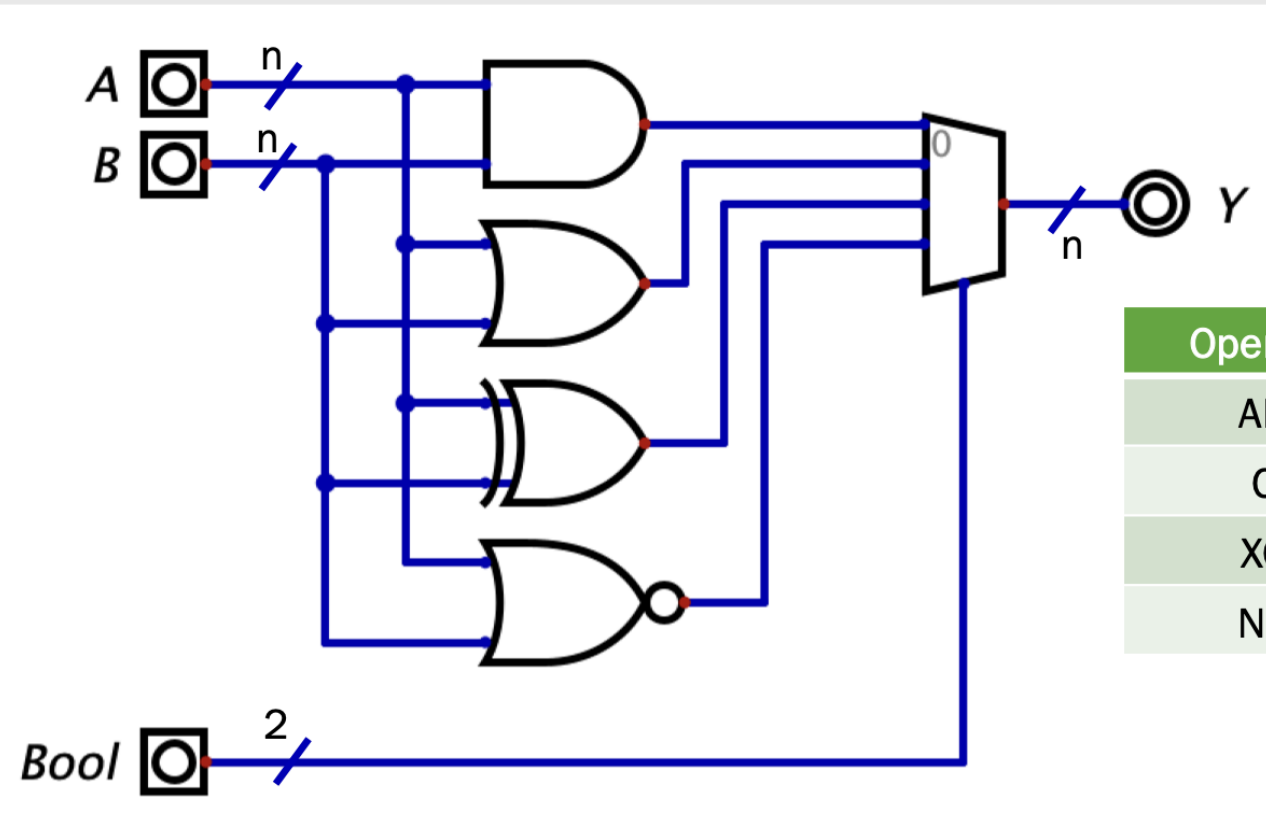
Lecture 14: Registers, Timing Analysis

tinyurl.com/comp311-fa25

Quiz Topics!

- K-maps (review!)
- Multiplexers (review!)
- Adder/Subtractor Circuits
- Shifter Circuits
- Comparator Circuits
- Tracing through an ALU
- Timing / Waveform Diagrams
 - *With propagation delay*
- Circuit design!
 - *Given a specification, implement a familiar circuit using known components*
 - *Familiarity with circuits we have designed together in class, in the labs*
 - *given a new control table for the ADD/SUB, SHIFT, or BOOL units, you should be able to re-wire it accordingly*

Boolean Unit



Operation	Expression	Bool
AND	$A \times B$	0b00
OR	$A + B$	0b01
XOR	$A \oplus B$	0b10
NOR	$\overline{A + B}$	0b11

Multiplexers Review

Multiplexers Review

- Create a 4:1 multiplexer out of 2:1 multiplexers.

A

B

C

D

S_1

S_0

S1	S0	Y
0	0	A
0	1	B
1	0	C
1	1	D

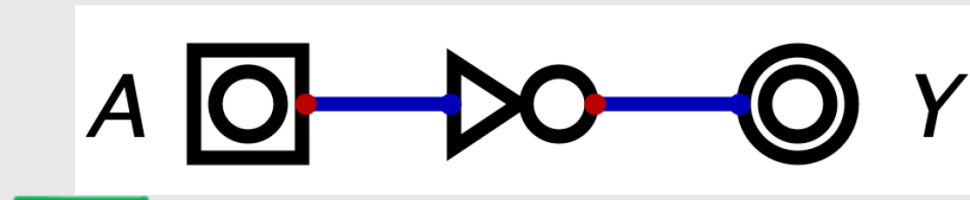
Y



PROPAGATION DELAY

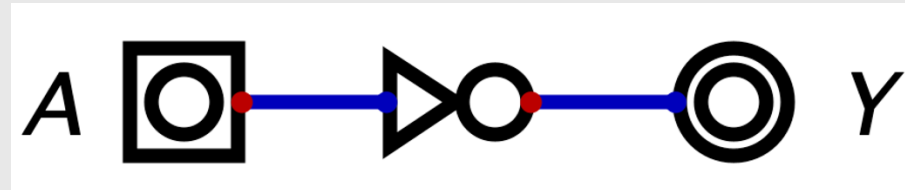
Propagation delay (t_{pd})

- When we change the input to this inverter, the output will not change immediately.
- There will be a delay before the output changes



Propagation delay (t_{pd})

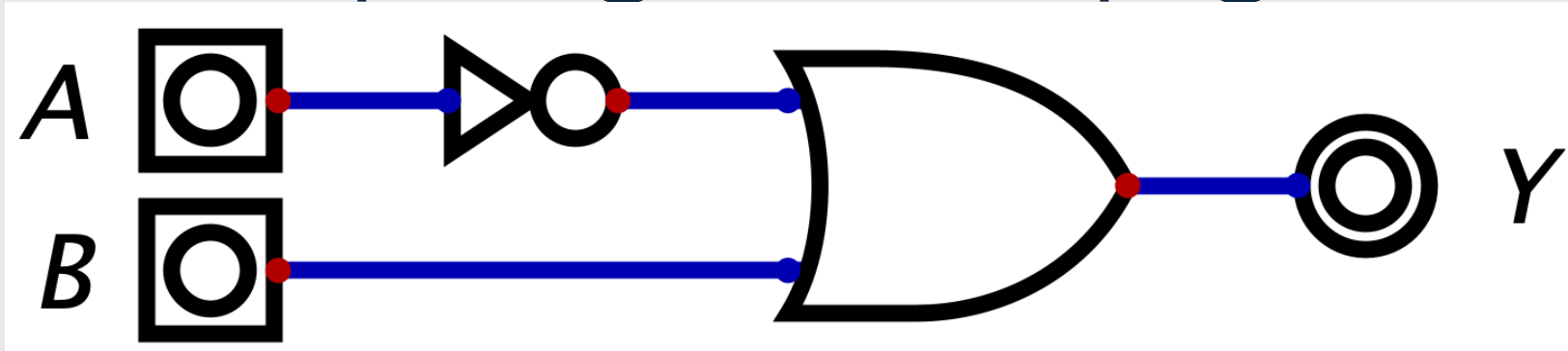
- Let's say the input to this inverter starts at 0.
- When we change the input to 1, the output will not become 0 immediately. There will be a delay.



A: 0 $\Rightarrow$ 1

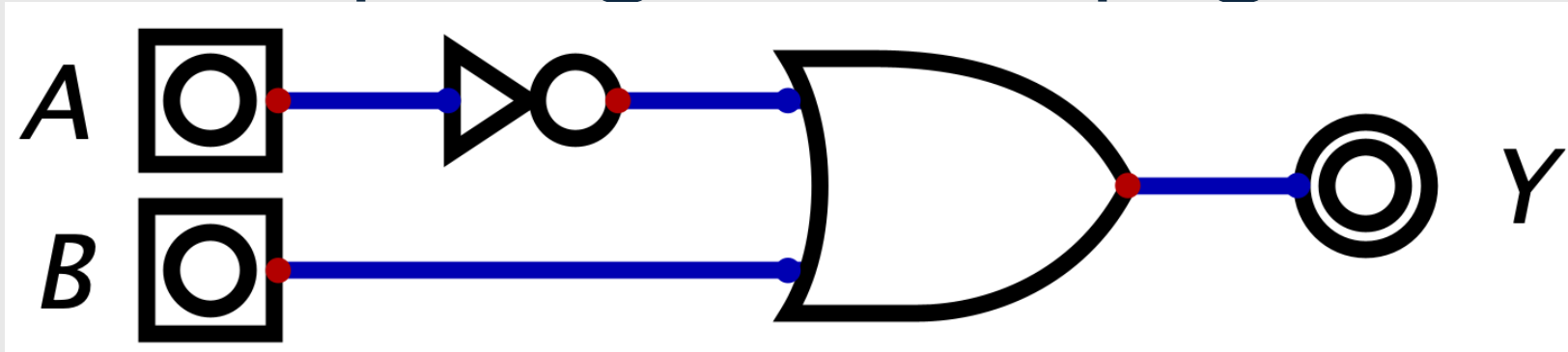
Y: 1 $\Rightarrow$ 0

Ex1: Computing Total Propagation Delay



Gate	t_{pd} (ps)
NOT	10
OR	20

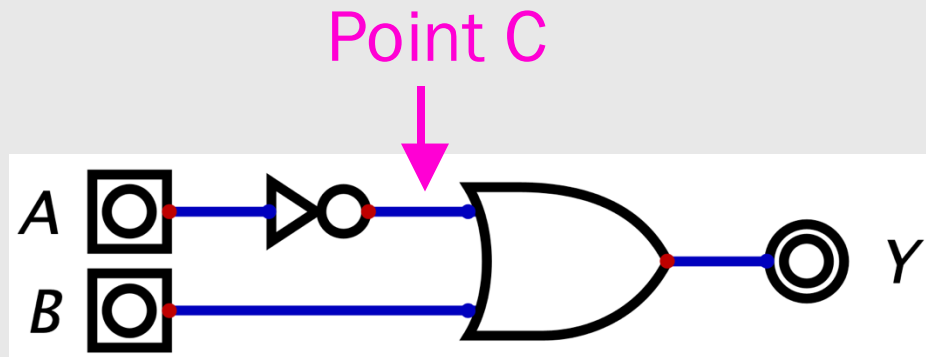
Ex1: Computing Total Propagation Delay



Gate	t_{pd} (ps)
NOT	10
OR	20

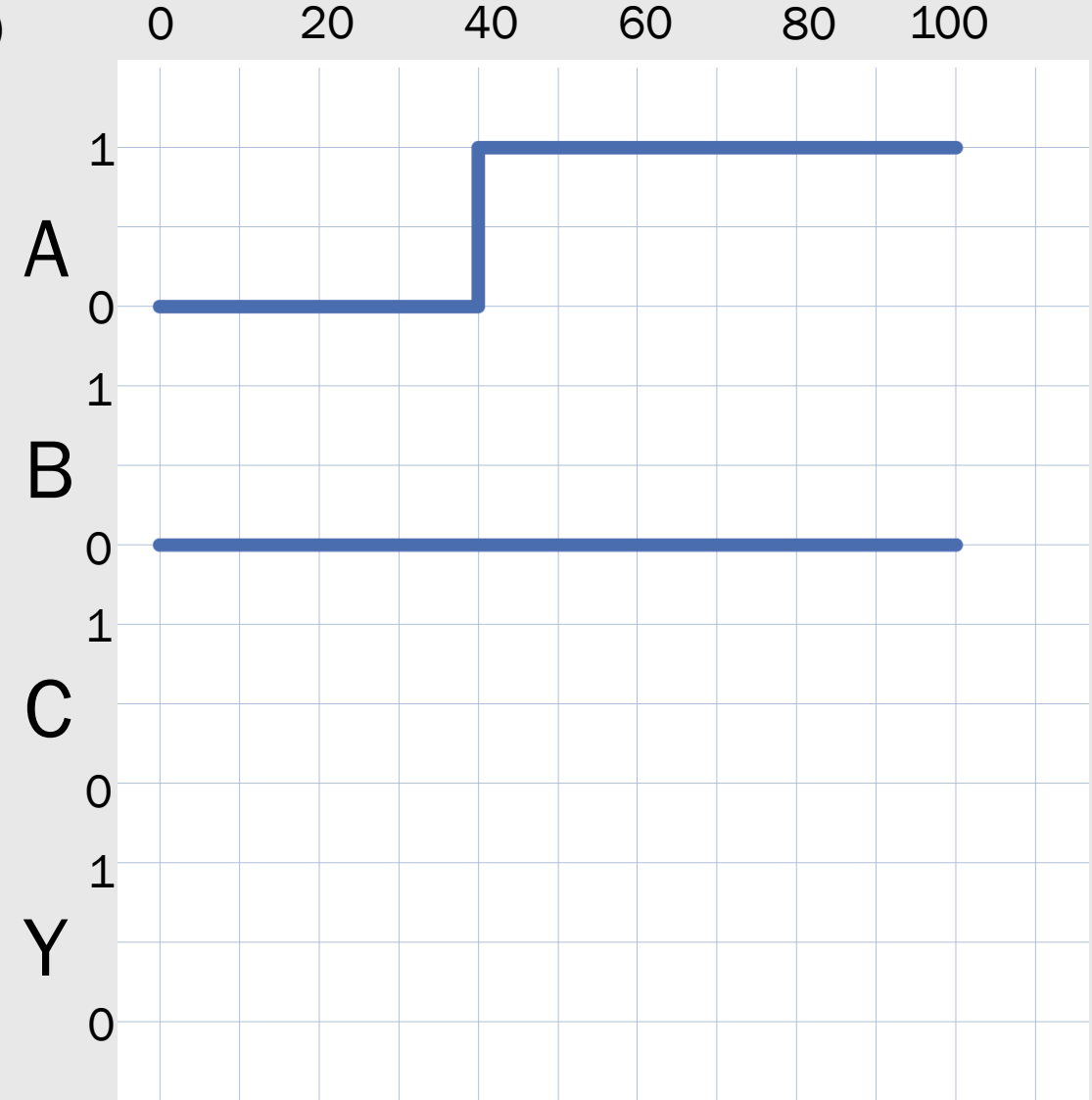
Delay from A to Y = 10ps + 20ps = 30ps
Delay from B to Y = 20ps

Ex1: Waveform Diagram with Propagation Delay

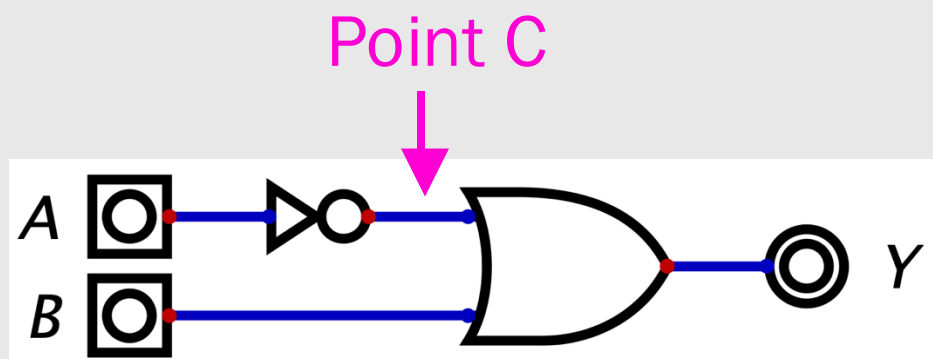


Gate	t_{pd} (ps)
NOT	10
OR	20

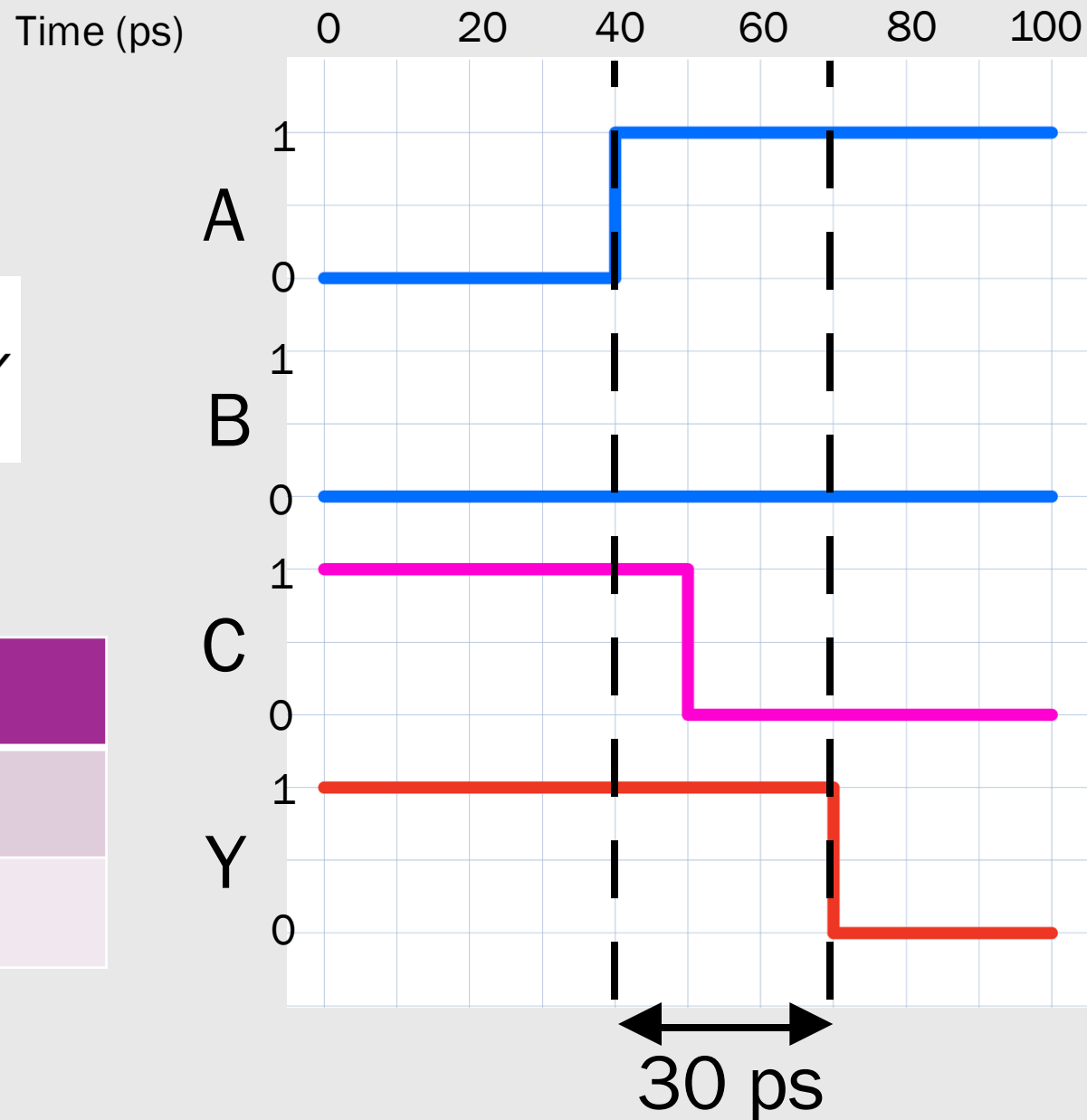
Time (ps)



Ex1: Waveform Diagram with Propagation Delay

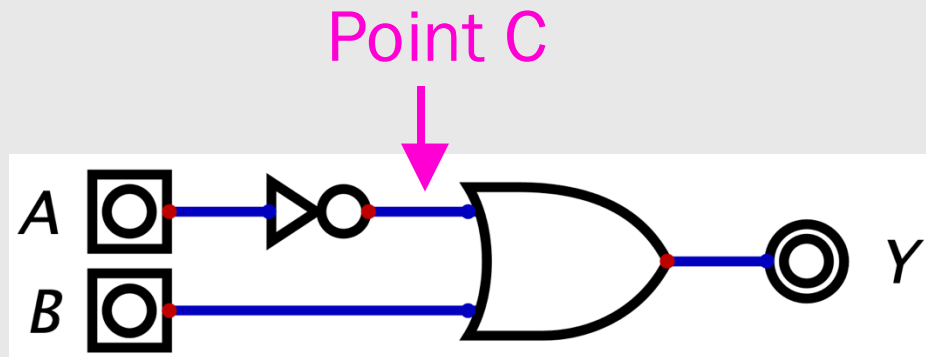


Gate	t_{pd} (ps)
NOT	10
OR	20



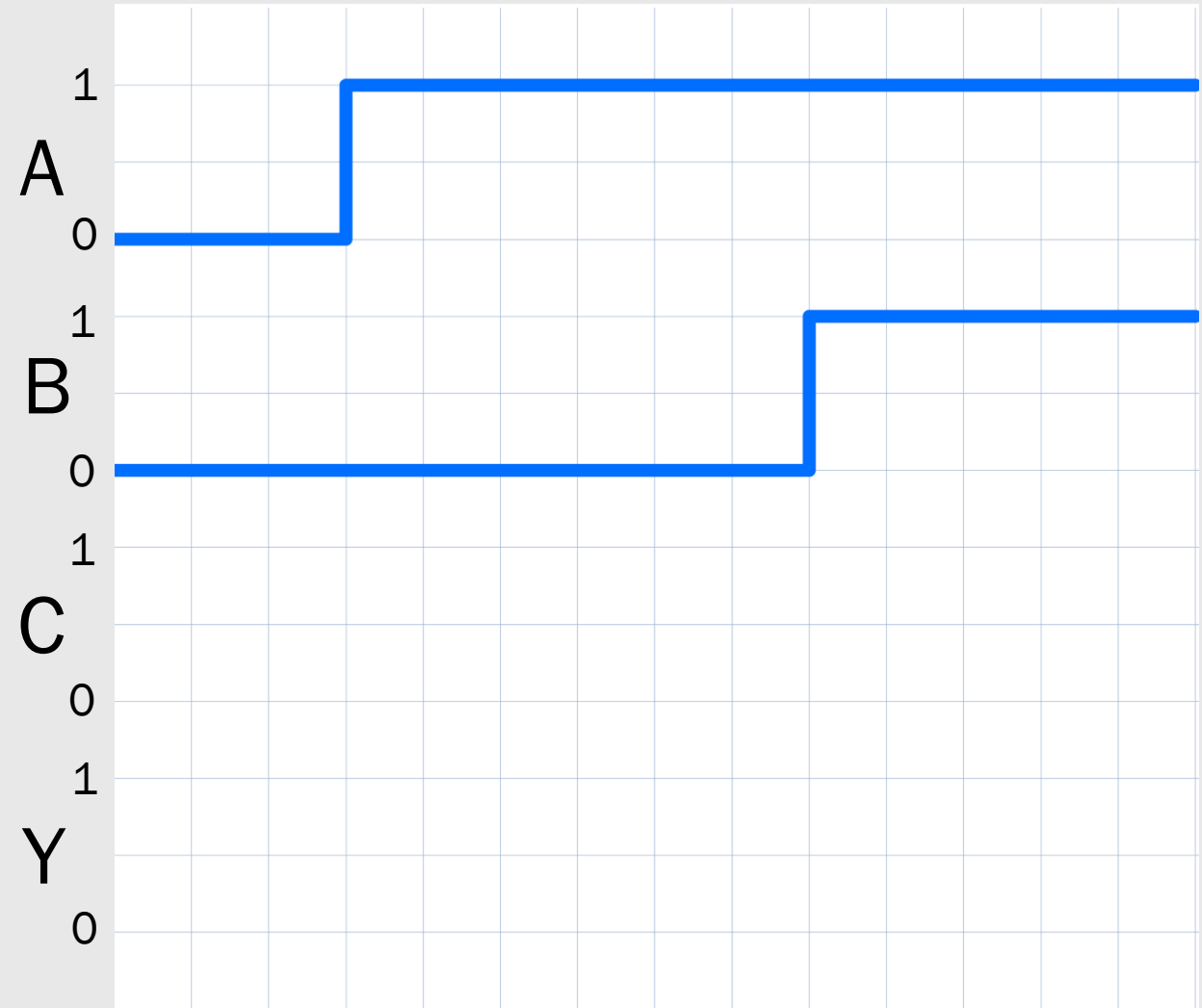
Ex2: Waveform Diagram with Propagation

Delay

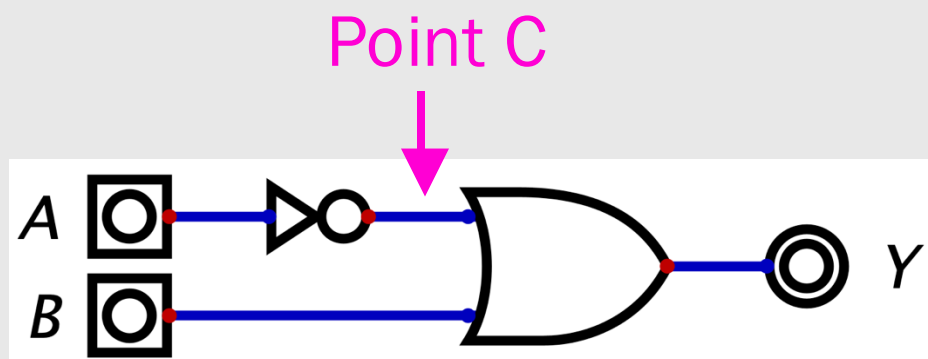


Gate	t_{pd} (ps)
NOT	10
OR	20

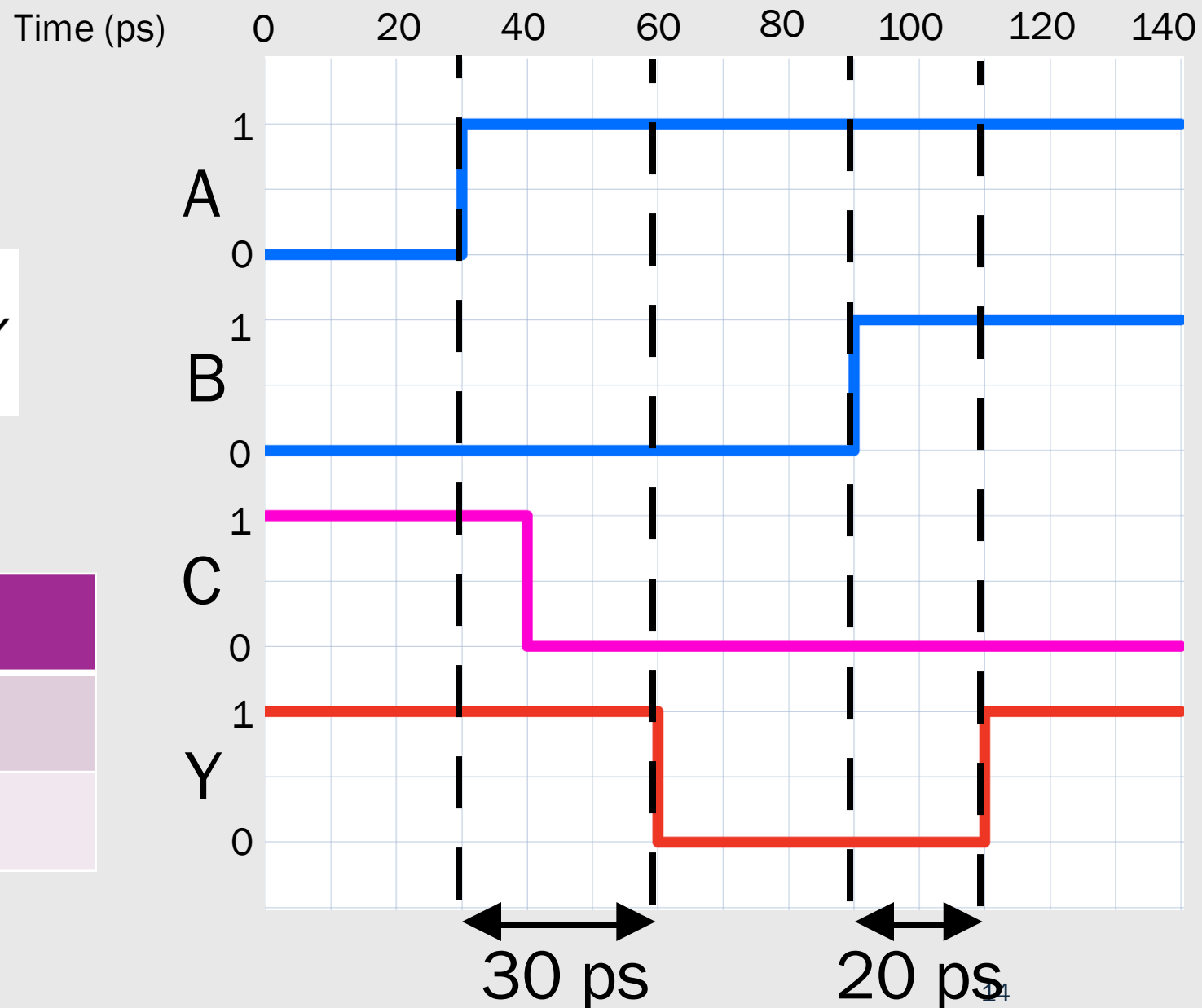
Time (ps) 0 20 40 60 80 100 120 140



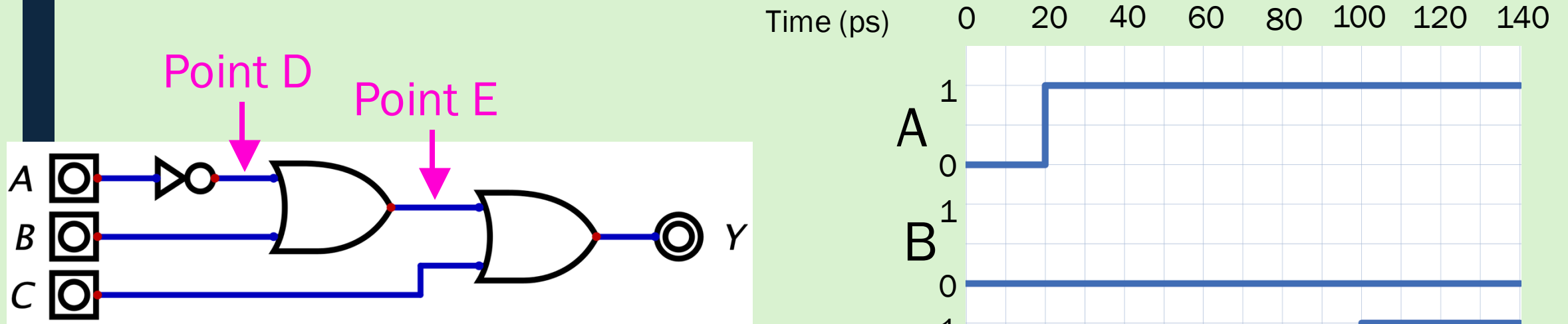
Ex2: Waveform Diagram with Propagation Delay



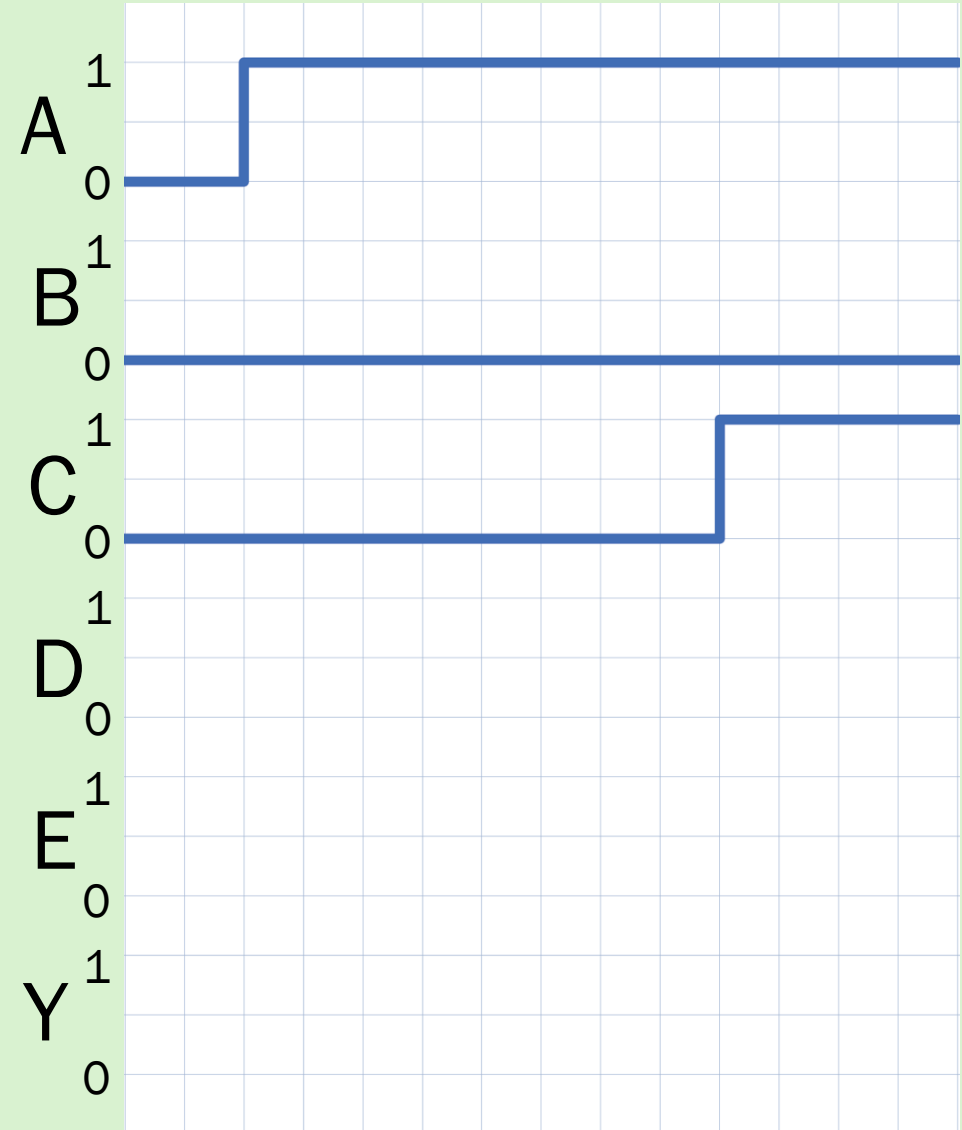
Gate	t_{pd} (ps)
NOT	10
OR	20



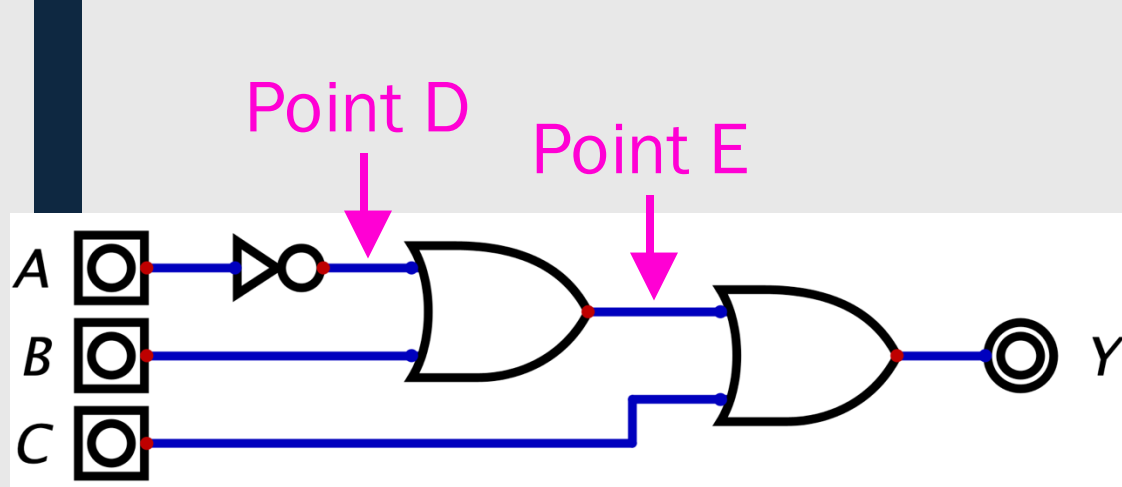
Waveform Diagram with Propagation Delay



Gate	t_{pd} (ps)
NOT	10
OR	30

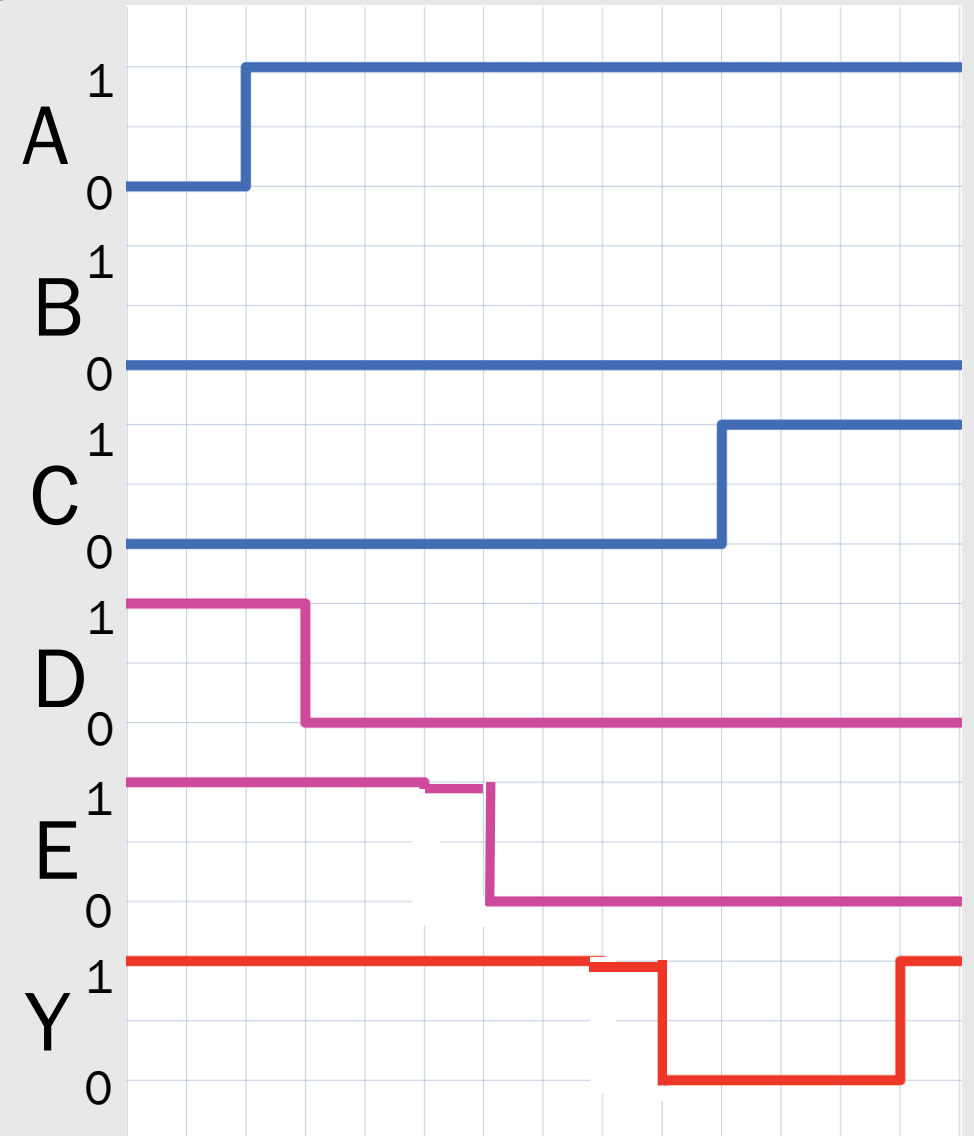


Waveform Diagram with Propagation Delay



Gate	t_{pd} (ps)
NOT	10
OR	30

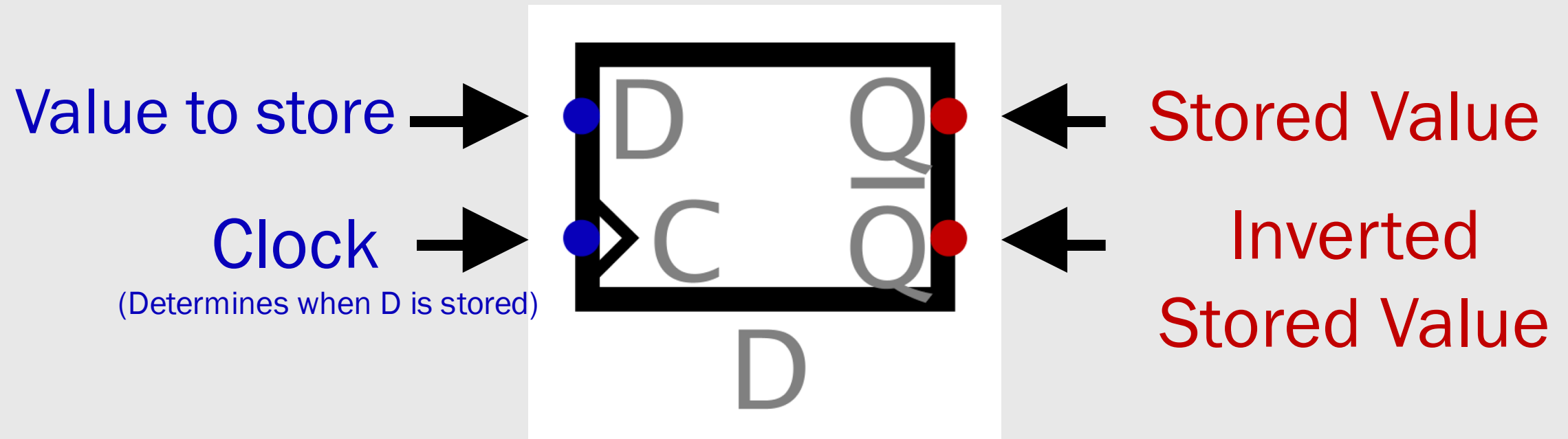
Time (ps) 0 20 40 60 80 100 120 140





FLIP FLOPS AND REGISTERS

D Flip-Flop

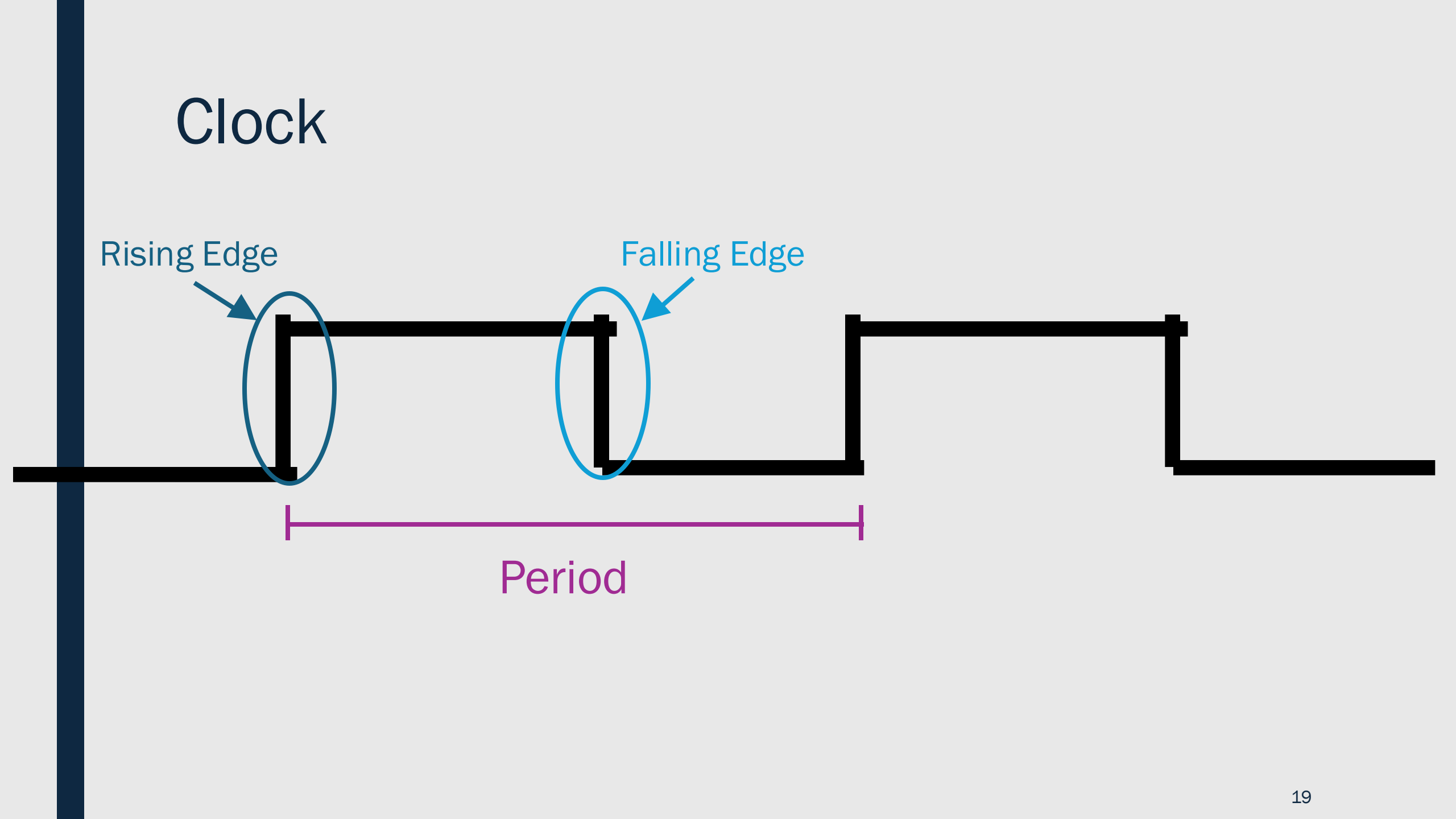


Clock

Rising Edge

Falling Edge

Period



Clock

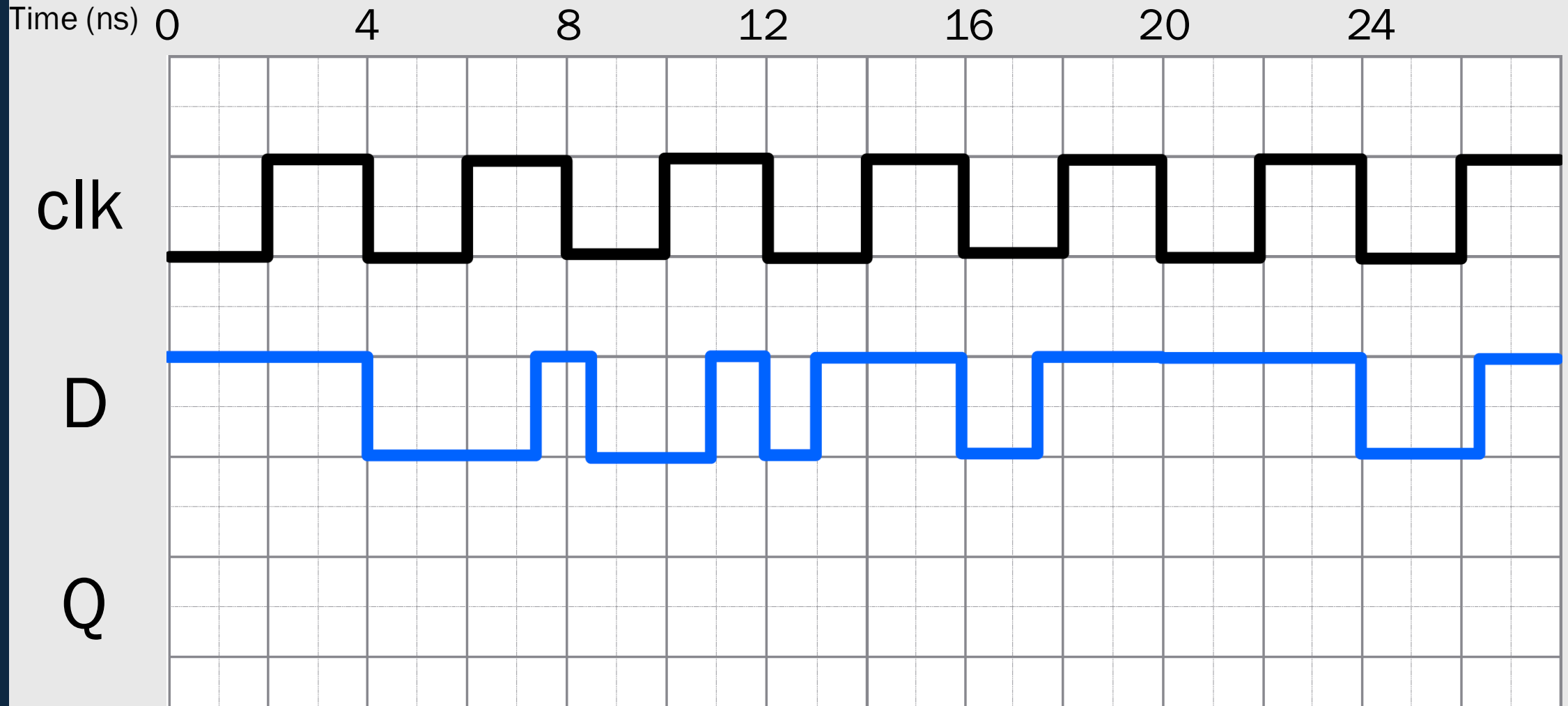
- The clock is a one-bit signal that oscillates (or toggles) back and forth between 0 and 1
- The purpose of the clock is to ensure that our circuits stay in sync
- The period of the clock is the time between one rising edge to the next. The clock spends an equal time in low and high states.
 - *The period determines how fast our circuit runs*
 - *The shorter the period – or in other words the higher the frequency – the faster our circuit will run*

D Flip-Flop

- Positive-edge triggered
 - *Stores D when the clock goes from 0 to 1*
- Negative-edge triggered
 - *Stores D when the clock goes from 1 to 0*

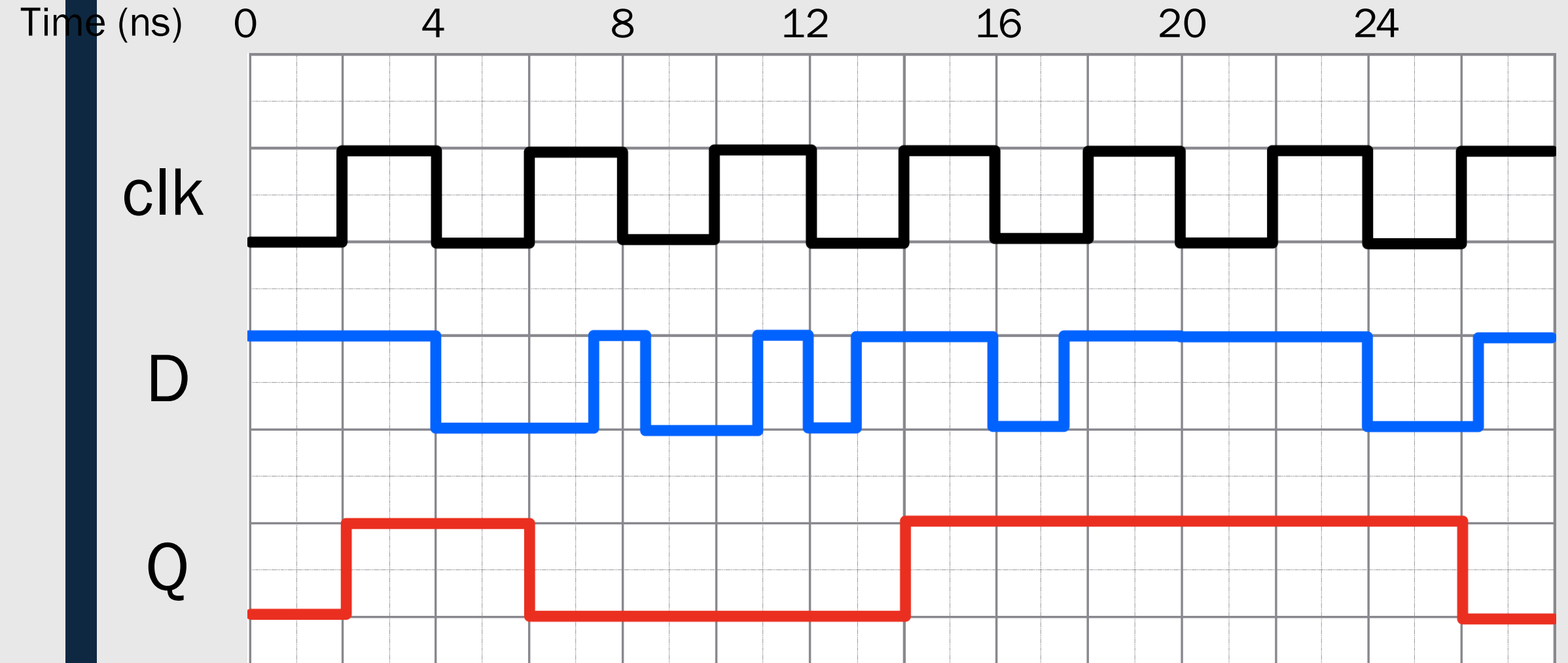


Positive Edge Triggered D Flip-Flop Waveform Diagram



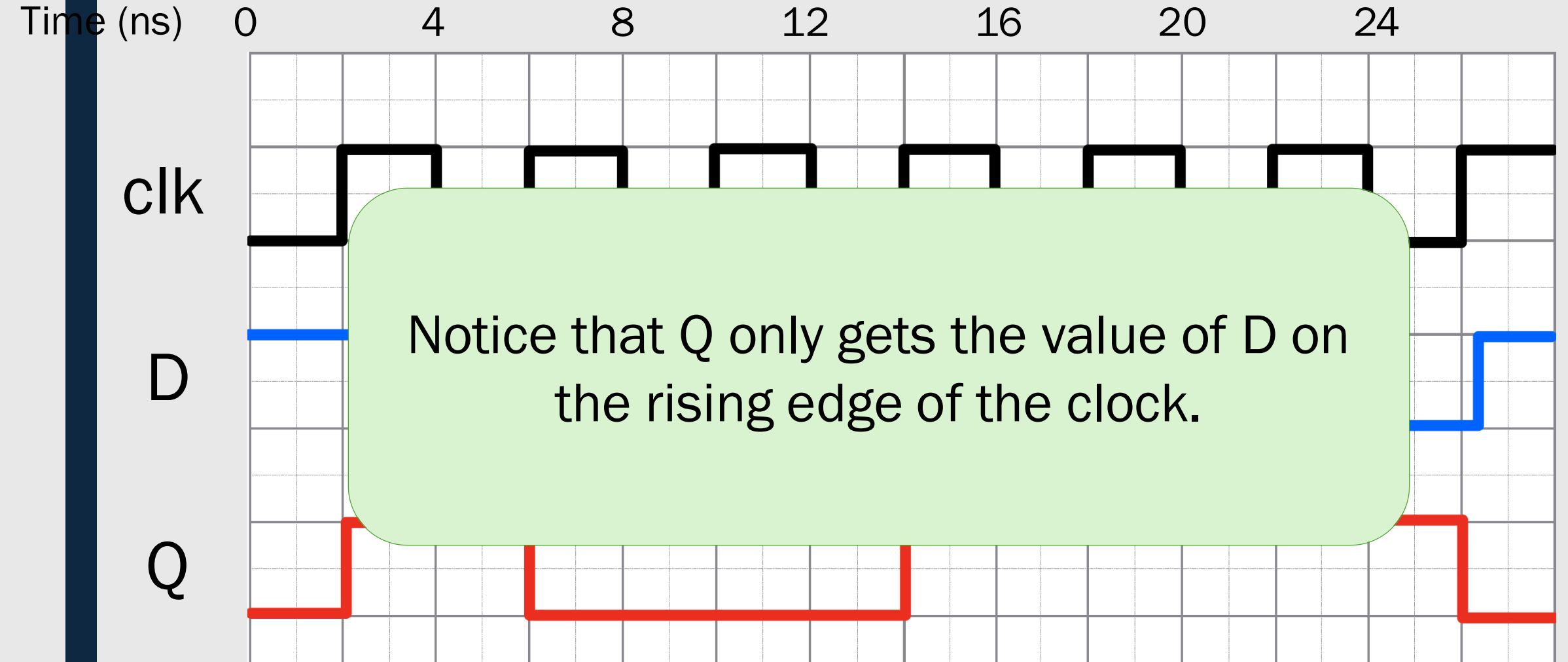
assume Q starts at 0

Positive Edge Triggered D Flip-Flop Waveform Diagram



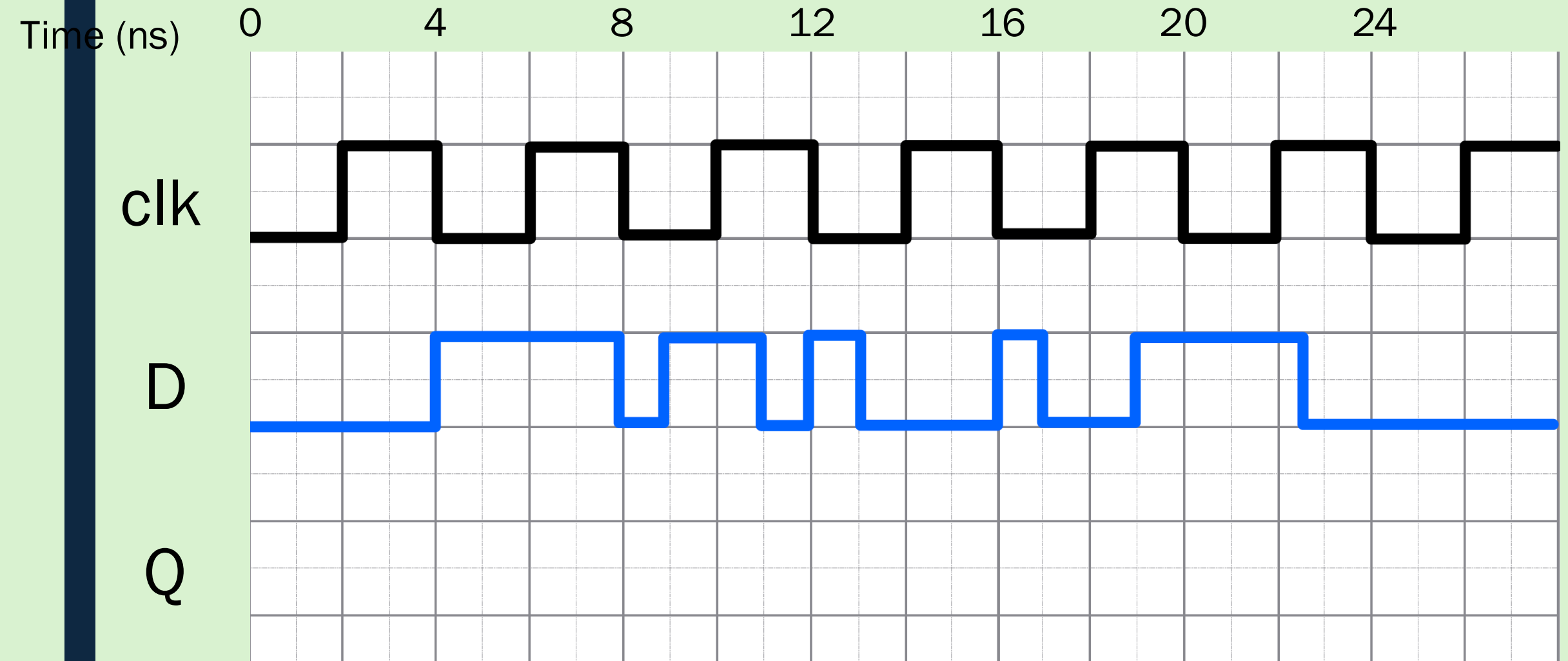
assume Q starts at 0

Positive Edge Triggered D Flip-Flop Waveform Diagram



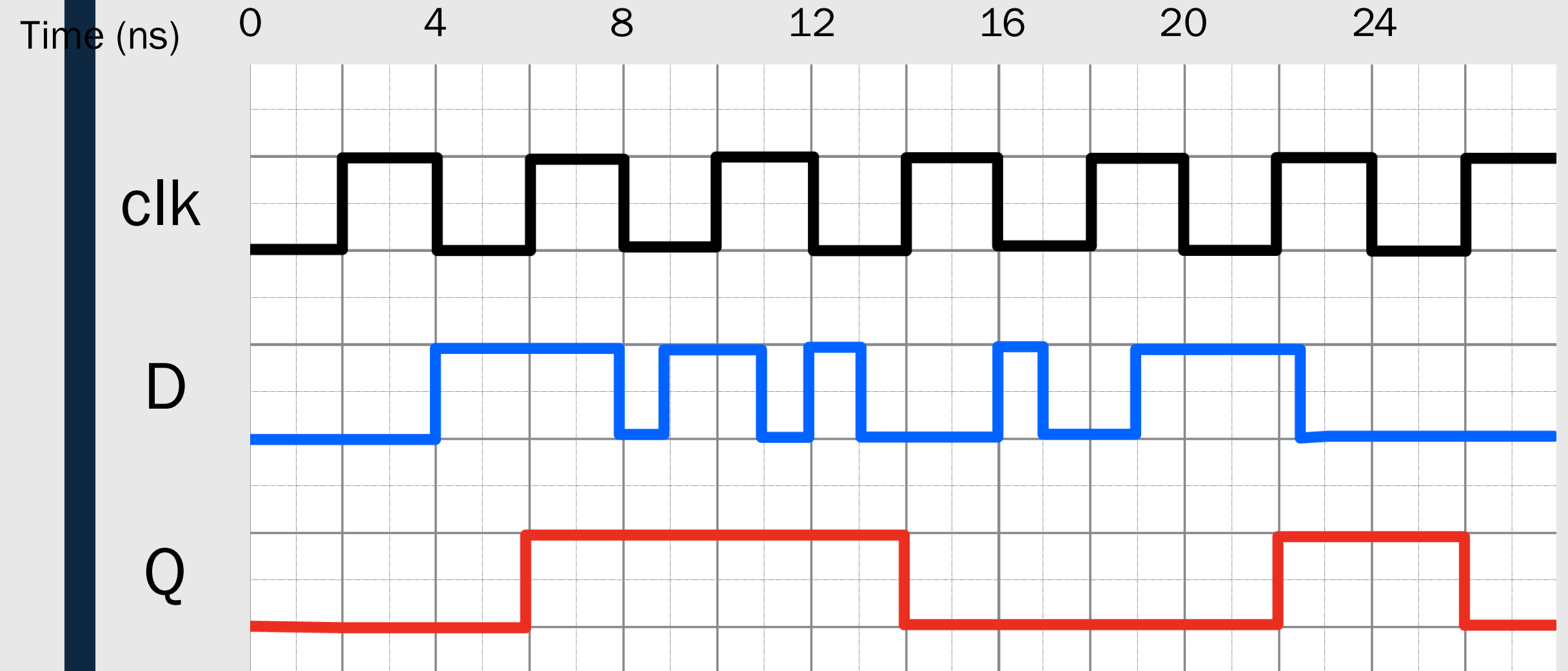
assume Q starts at 0

Positive Edge Triggered D Flip-Flop Waveform Diagram



assume Q starts at 0

Positive Edge Triggered D Flip-Flop Waveform Diagram



assume Q starts at 0