

pollev.com/kakiryan

COMP311: *COMPUTER ORGANIZATION!*

Lecture 21: I-Type Instructions!

tinyurl.com/comp311-fa25



RISC-V ASSEMBLY! 😊
YAY YAY YAY FUN FUN

Reminder: How are programs turned into machine code?

High-level language

→ `c = a + b`



Assembly



`add x5, x4, x3`



Machine Code



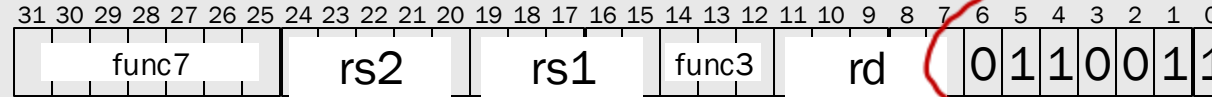
`000000000011001000000001010110011`

The miniRISC-V ISA

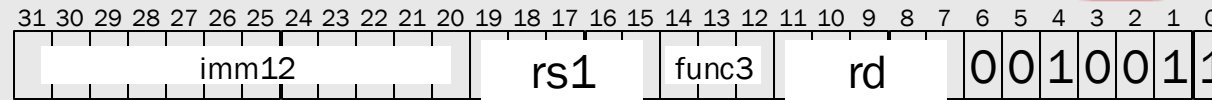
32-bit



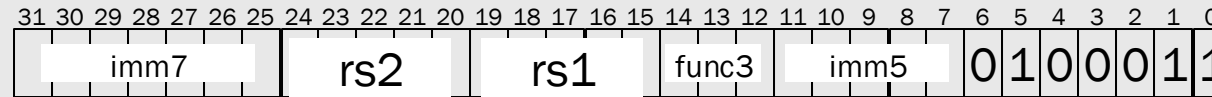
R-type:



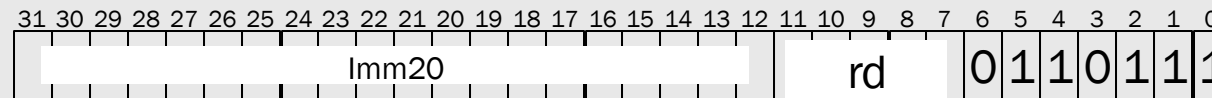
I-type:



B/S-type:



U-type:



Four key instruction formats (each one has a corresponding opcode!):

- 1) ALU with two register operands
- 2) ALU with a register and an immediate operand
- 3) Stores and Branches
- 4) Jumps and large constants (LUI, AUIPC)

R-format vs I-format Instructions

- R-format

- *Used for operations between two registers*

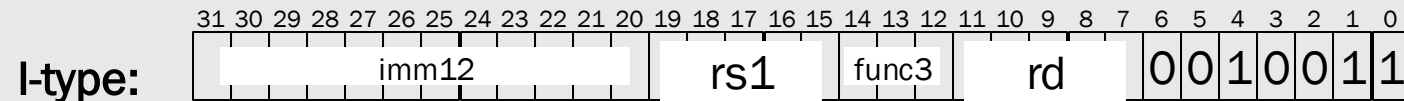
- I-format

- *Used for operations between a register and an immediate value*

- in other words, if you want to use a constant that is not in a register

I-type Data Processing

Instructions that process one register and a constant:



Notice there is no SUBI instruction. Why?



000 - ADDI
001 - SLLI
010 - SLTI
011 - SLTUI
100 - XORI
101 - SRLI/SRAI
110 - ORI
111 - ANDI



andi **x5**, **x10**, **255**

I-type instructions
have the following template:

OPfunc3 **rd**, rs1, imm12

Is encoded as:

0000	1111	1111	0101	0111	0010	1001	0011
------	------	------	------	------	------	------	------

0x0ff57293

I-Format Syntax

op rd, rs1, immediate12



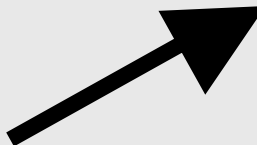
this is where we will store
the result of the operation

I-Format Syntax

$$x5 = x4 + 12$$

addi x5, x4, 12

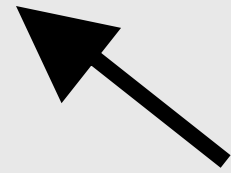
destination
register (rd)



source
register
(rs1)



immediate
value



R-Format vs I-Format Syntax

R-Format

op rd, rs1, rs2

$R[rd] = R[rs1] \text{ op } R[rs2]$

writes to rd

I-Format

op rd, rs1, immediate

$R[rd] = R[rs1] \text{ op immediate}$

writes to rd

Register 0

- Register 0 always holds the value 0
- This is very useful when we want to write a constant value to a register

Example Program

a = 5

b = 3

c = a + b

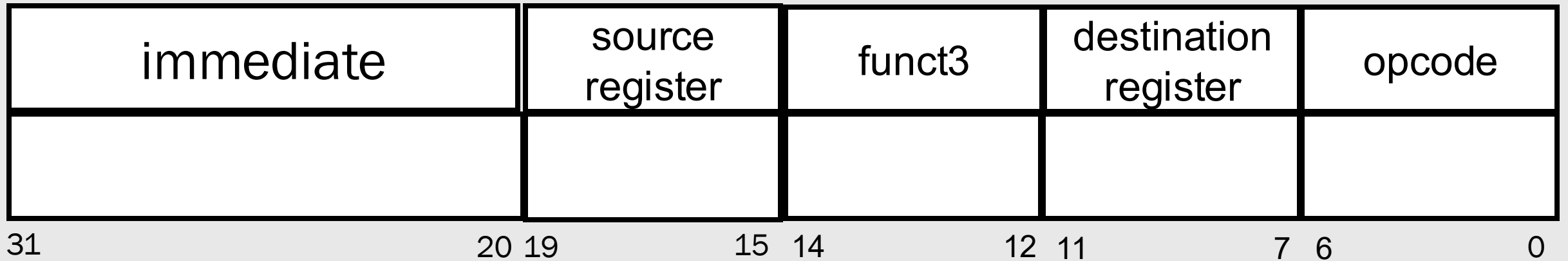
addi x10, x0, 5

addi x11, x0, 3

add x12, x10, x11

I-Format Syntax

addi x5, x0, 12



I-Format Syntax

addi x5, x0, 12

immediate							source register			funct3			destination register				opcode			
0000 0000 1100							00000			000			00101				0010011			
31						20	19		15	14		12	11		7	6				0

I-type Data Processing

ALU instructions with a register and an immediate operand

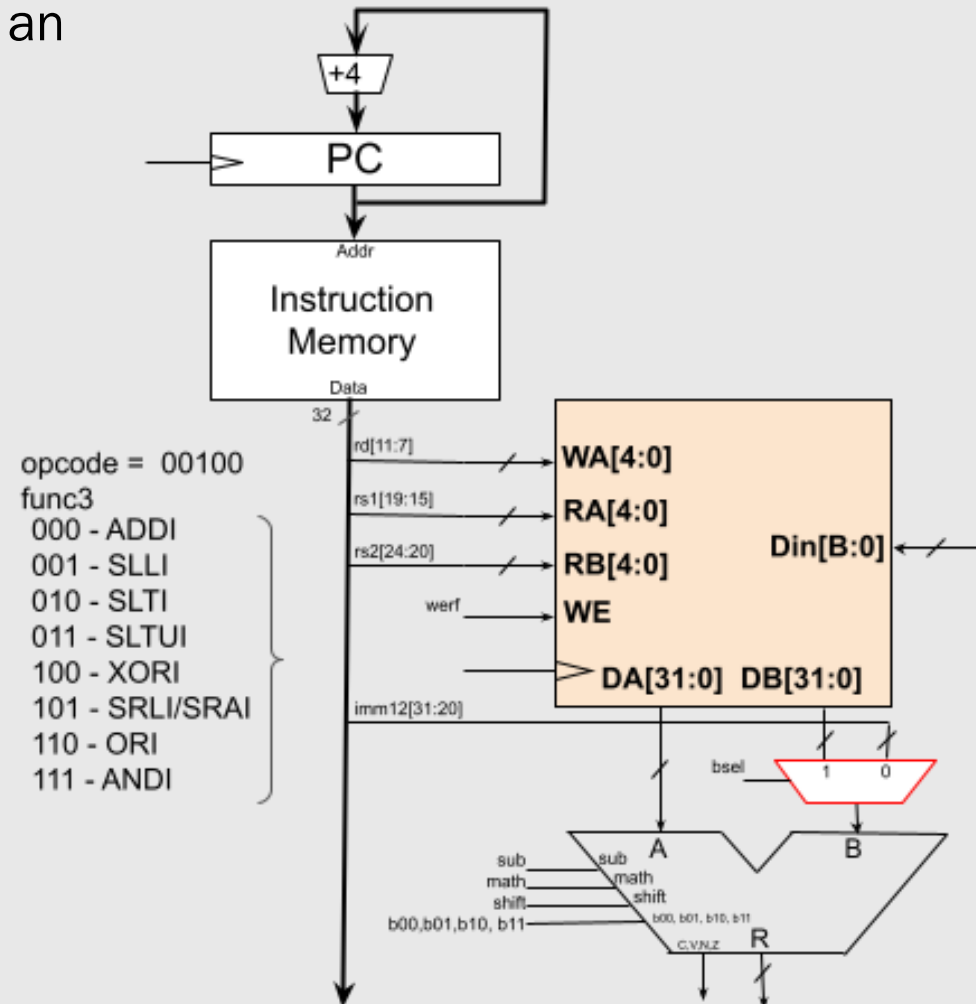
Rd - register file write address

Rs1 - register source operand

Imm12 - 12-bit immediate operand

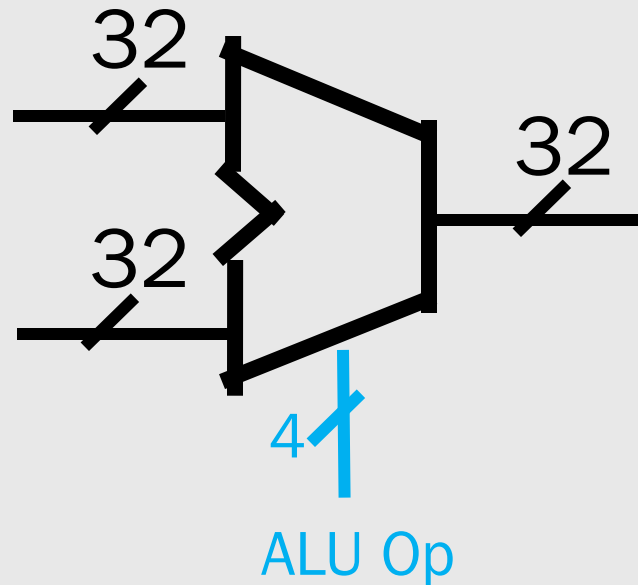
Adds a mux to the B input of the ALU

- 12-bit immediate value is sign-extended 20-bits



Bit Extension

- The ALU operates on 32-bit values
- We need to extend the immediate value to make it compatible with the ALU



Logical Operations: Zero Extend Immediate

16 bits

$A = A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$

32 bits

$A = 0000000000000000 A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$

Arithmetic Operations: Sign Extend Immediate

16 bits

$$A = A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$$

32 bits

$$A = \underbrace{A_{15} A_{15} A_{15} A_{15} A_{15} A_{15} A_{15} A_{15} A_{15} A_{15} A_{15} A_{15} A_{15} A_{15} A_{15}}_{\text{Sign Extension}} A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0$$

Sign Extension Preserves the Value

16 bits

A = 1111111111111011

A = -5

32 bits

A = 11111111111111111111111111111011

A = -5

Zero Extension Changes Negative Values

16 bits

A = 1111111111111011

A = -5

32 bits

A = 00000000000000001111111111111011

A = 65531

Instruction Operations

op rd, rs, immediate

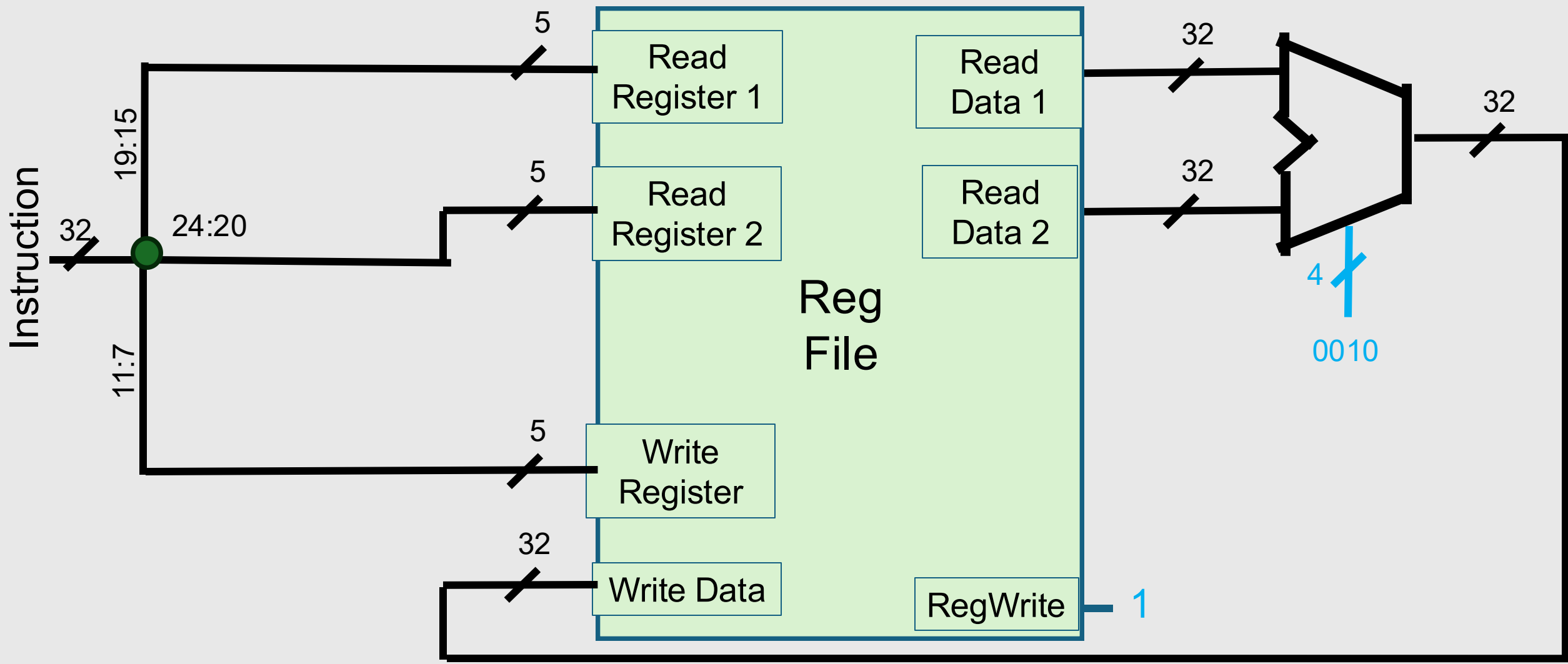
Name	Operation
addi	
andi	
ori	
slti	

Instruction Operations

op rd, rs1, immediate

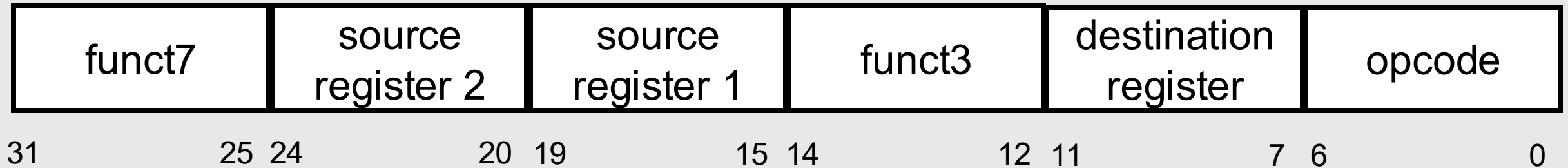
Name	Operation
addi	$\text{Reg}[\text{rd}] \leftarrow \text{Reg}[\text{rs1}] + \text{sign_extend}(\text{imm12})$
andi	$\text{Reg}[\text{rd}] \leftarrow \text{Reg}[\text{rs1}] \& \text{sign_extend}(\text{imm12})$
ori	$\text{Reg}[\text{rd}] \leftarrow \text{Reg}[\text{rs1}] \text{sign_extend}(\text{imm12})$
slti	$R[\text{rd}] = (R[\text{rs1}] < \text{SignExtImm}) ? 1 : 0$

Original Datapath

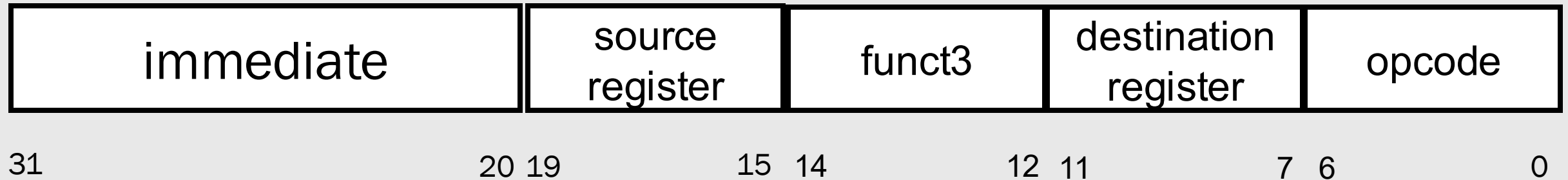


R-Format vs I-Format Instructions

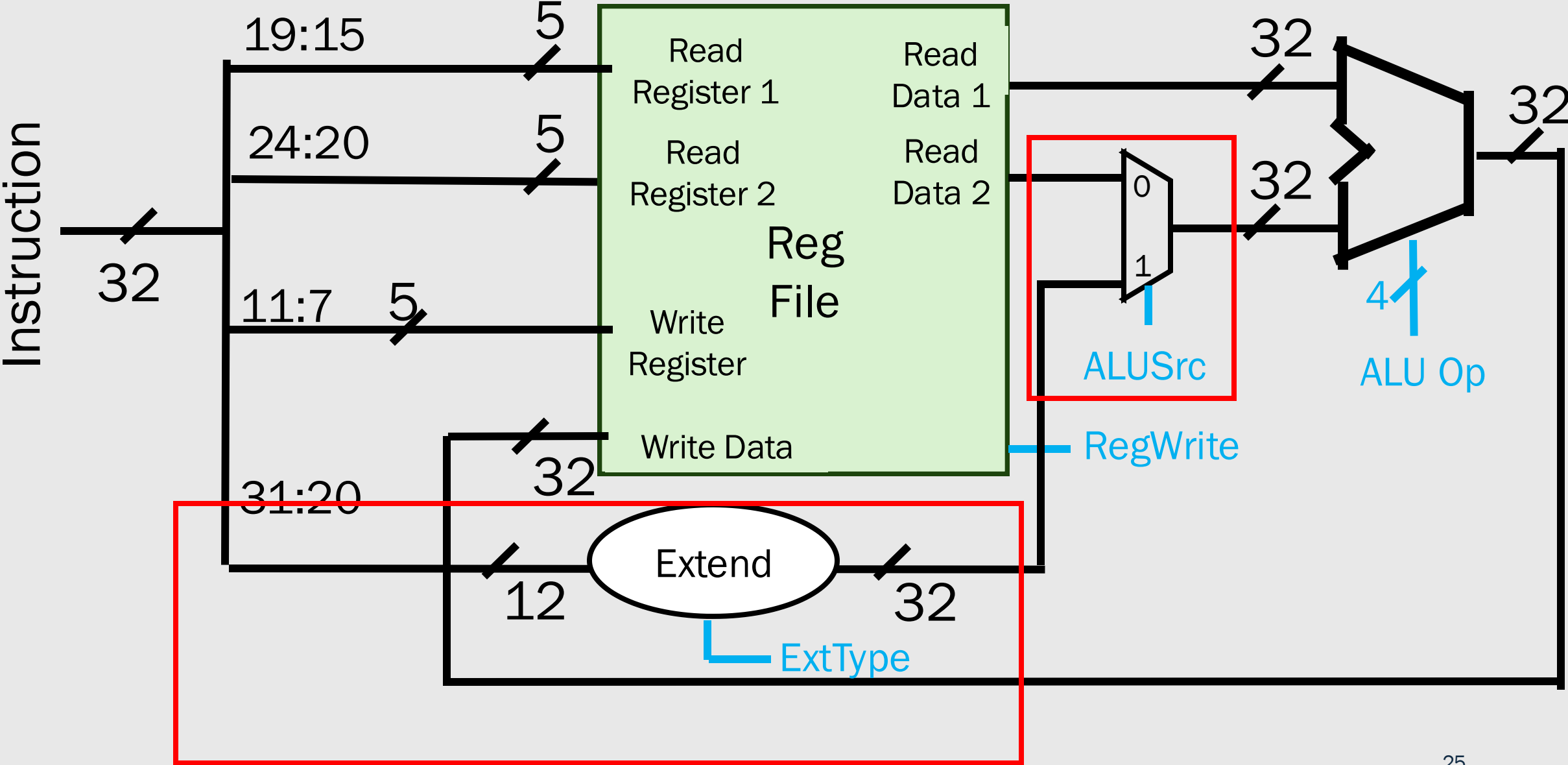
R-Format



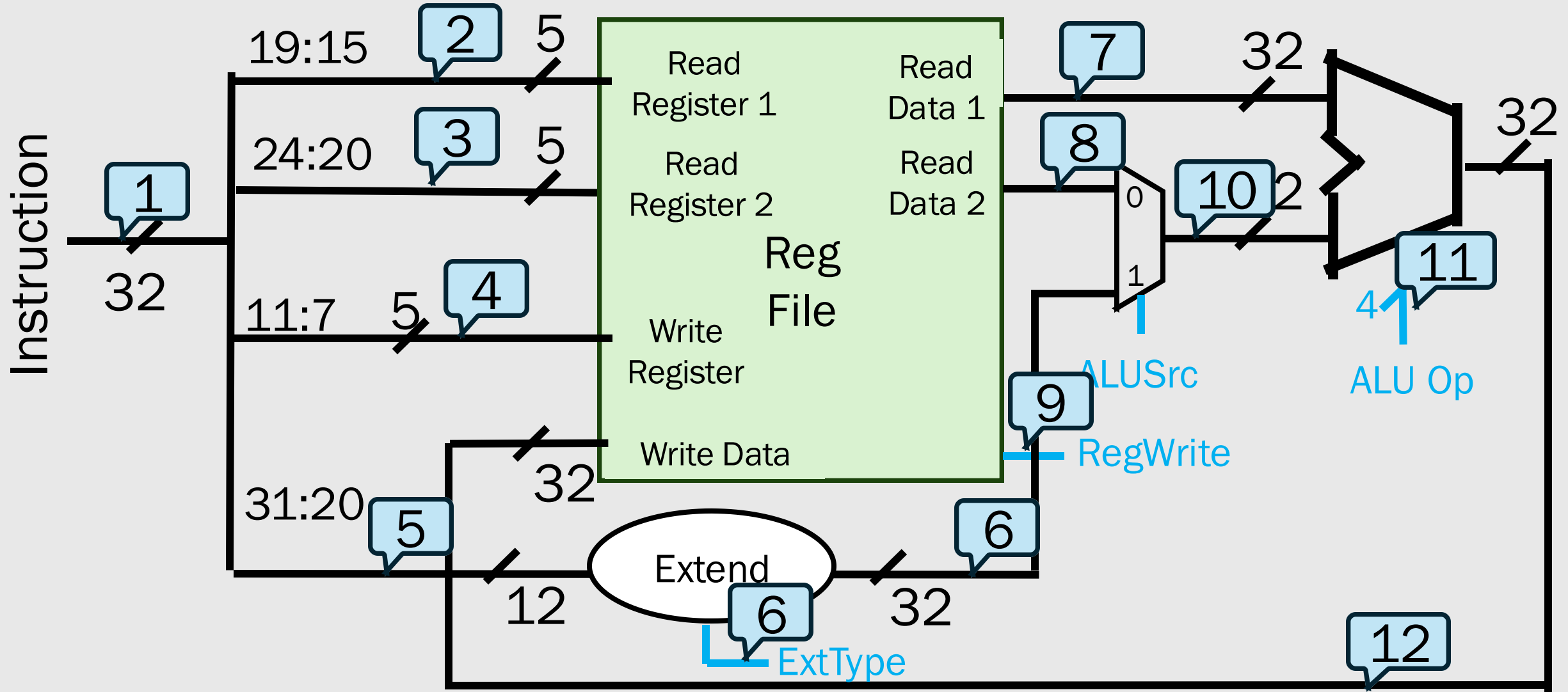
I-Format



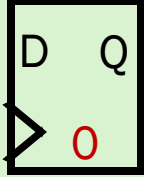
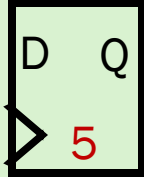
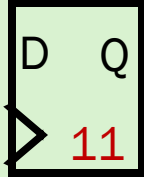
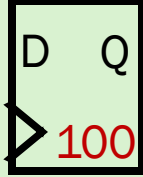
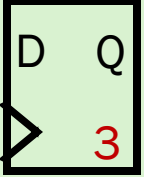
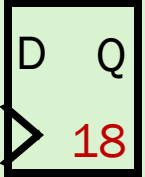
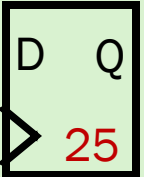
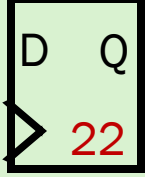
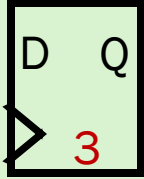
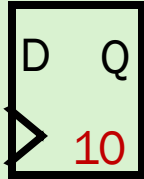
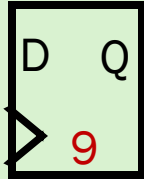
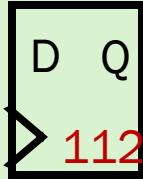
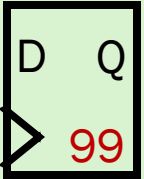
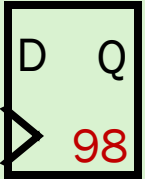
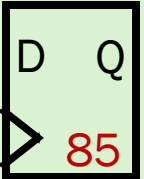
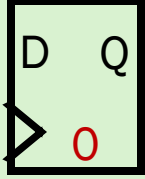
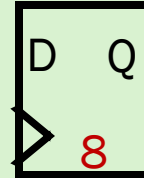
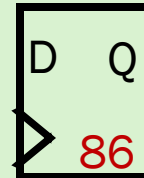
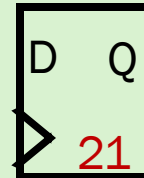
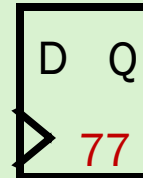
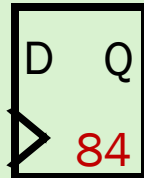
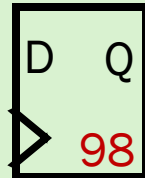
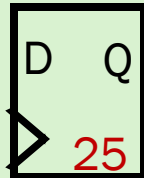
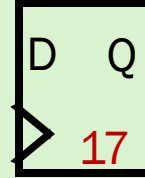
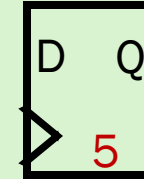
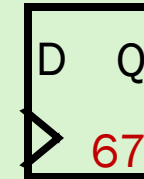
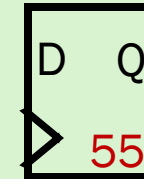
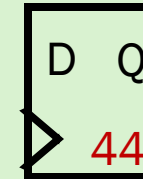
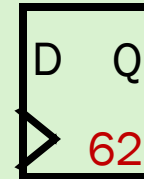
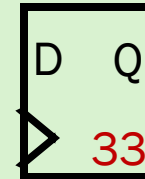
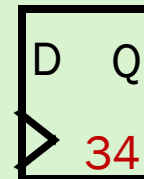
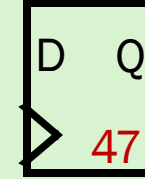
Hardware Support for I-Format Instructions



What is the value of each signal when executing `ori x4, x5 20`?



Contents of RegFile

Reg 0	Reg 1	Reg 2	Reg 3	Reg 4	Reg 5	Reg 6	Reg 7
							
Reg 8	Reg 9	Reg 10	Reg 11	Reg 12	Reg 13	Reg 14	Reg 15
							
Reg 16	Reg 17	Reg 18	Reg 19	Reg 20	Reg 21	Reg 22	Reg 23
							
Reg 24	Reg 25	Reg 26	Reg 27	Reg 28	Reg 29	Reg 30	Reg 31
							

What is the value of each signal when executing **ori x4, x5, 20**

immediate										source register					funct3			destination register					opcode			
31									20	19				15	14			12	11				7	6		0