COMP311 In-Class Practice 11/9/26 Name: _____

Question 1: Minimum Clock Period: Full Single-Cycle Datapath What is the minimum clock period that will work for all instructions in a single-cycle datapath? Assume a clk-to-q delay of 20ps. Use the timing tables below to help answer the question.

	Fetch	Decode	Execute	Memory	Writeback
Time	200ps	100ps	200ps	200ps	100ps

Instruction	Fetch	Decode	Execute	Memory	Writeback	Total Time
arithmetic and logical (add, addi, or, etc)	X	X	X		X	200ps + 100ps + 200ps + 100ps = 600ps
sw	X	X	X	X		200 + 100 + 200 + 200 = 700ps
lw	X	X	X	X	X	200 + 100 + 200 + 200 + 100 = 800ps
branch	X	X	X			200 + 100 + 200 = 500ps
j	X	X				200 + 100 = 300ps

Question 2: Performance Analysis 2.1. What is the minimum clock period for the pipelined, 5-stage implementation?

2.2. What is the latency of a single instruction in the single-cycle datapath, assuming the minimum clock period found above?

2.3. What is the latency of a single instruction in the pipelined, 5-stage implementation, assuming the minimum clock period found above?

2.4. What is the speedup of executing the following set of instructions on a single-cycle vs. the 5-stage pipelined implementation?

```
1 add x8, x6, x7
2 lw x9, 100(x0)
3 sub x8, x9, x20
4 sw x10, 0(x20)
5 or x21, x11, x12
```