11/2/26

COMP 311: *Computer Organization!*

Lecture 21: Register File mini Lab



The University of North Carolina at Chapel Hill

https://tinyurl.com/comp311-fa26

Logistics Update



- Lab 3 is out
  - Due tomorrow

Plan for Class Today



- 4:20-4:50: Building and Analyzing a Register File Implementation in Digital ☺

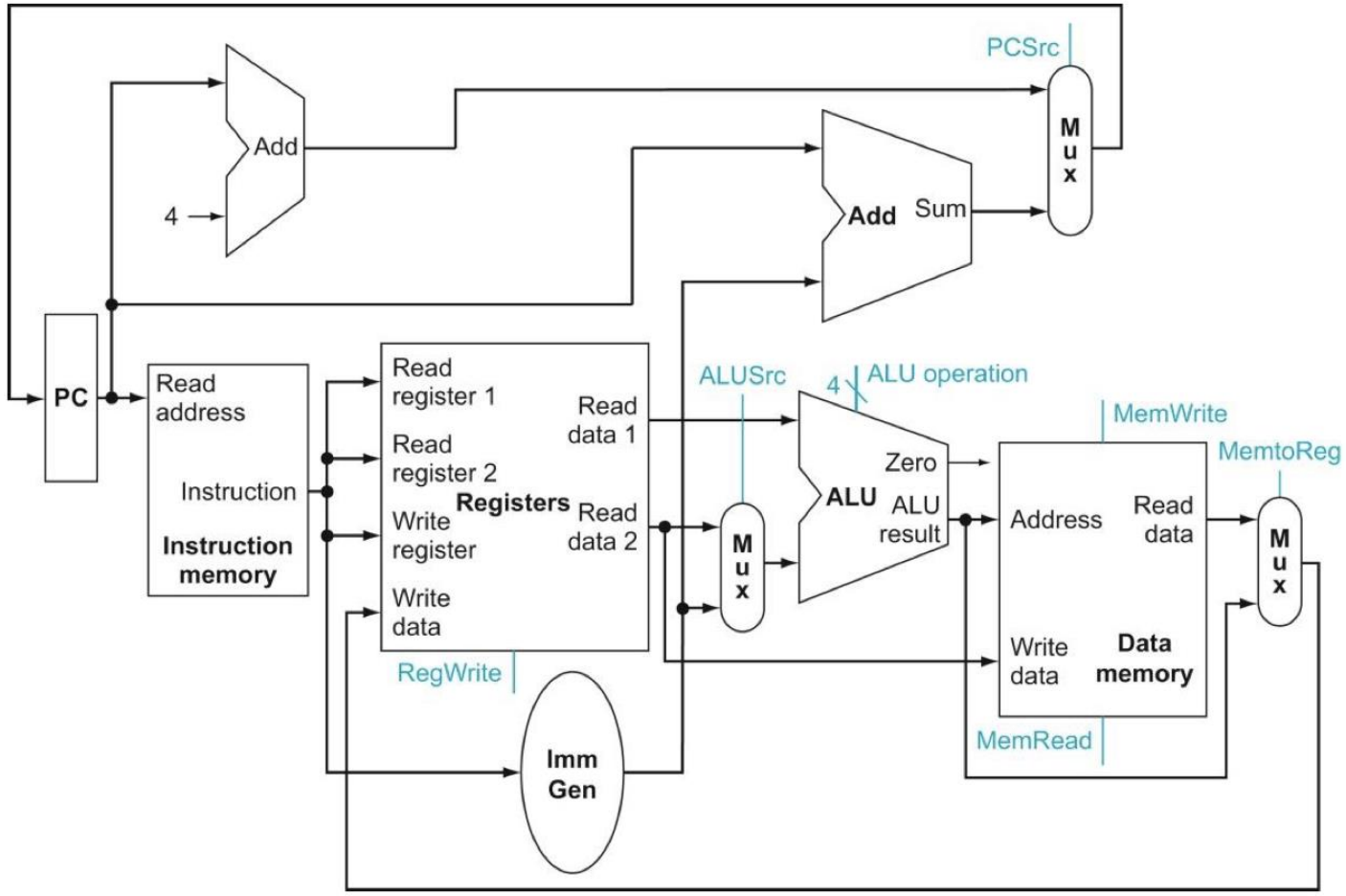
Guiding Question ☺

How does hardware remember information, and how can we predict when its outputs change?

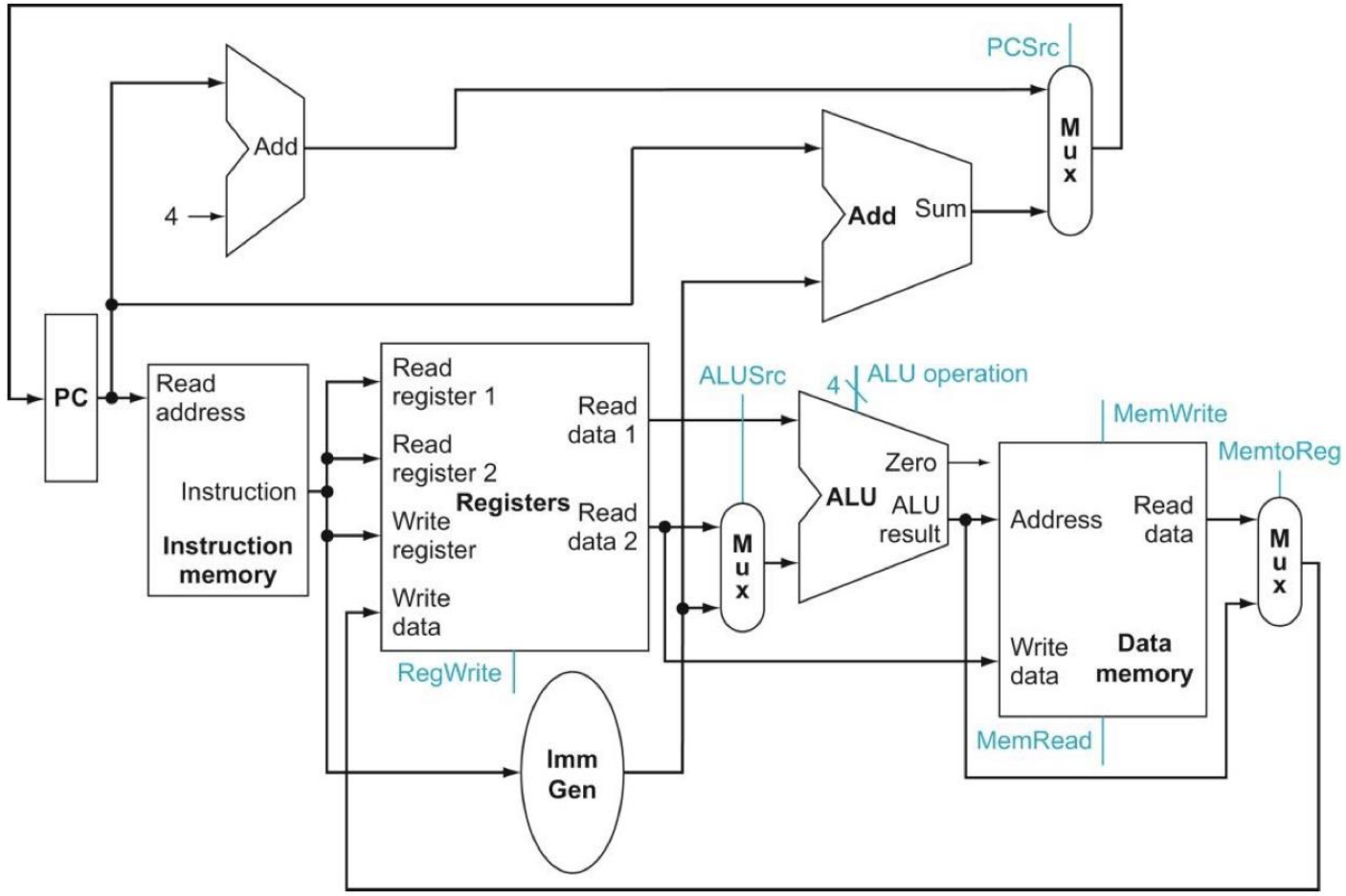


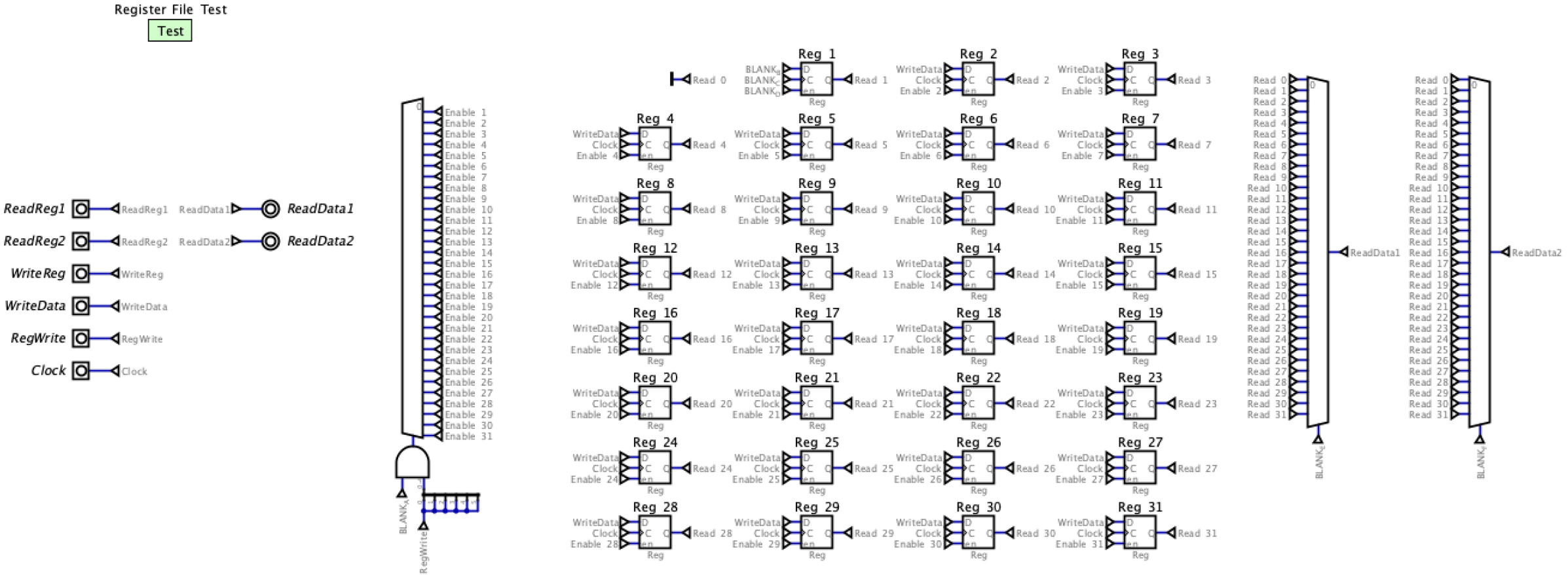
Review: The RISC-V Datapath

The RISC-V Datapath



Today: We will build a reusable register file!!




Register File Test
Test
ReadReg1
ReadReg2
WriteReg
WriteData
RegWrite
Clock
ReadData1
ReadData2
Reg 0
Reg 1
Reg 2
Reg 3
Reg 4
Reg 5
Reg 6
Reg 7
Reg 8
Reg 9
Reg 10
Reg 11
Reg 12
Reg 13
Reg 14
Reg 15
Reg 16
Reg 17
Reg 18
Reg 19
Reg 20
Reg 21
Reg 22
Reg 23
Reg 24
Reg 25
Reg 26
Reg 27
Reg 28
Reg 29
Reg 30
Reg 31

Q1: Some Planning…



- Work with a partner!
- Download the starter ZIP from today's course-page link.
- Unzip; open register-file.dig in Digital; stop simulation.
- Answer Q1

Q1: Some Planning…



- 32 register numbers; 32-bit values;
  - two reads and one write.
- Reads follow the selected register after the circuit settles.
- Writes occur on a rising clock edge when RegWrite = 1.
- x0 always reads as zero. Keep this component for your CPU.

Q2: six signal-name blanks

- A: below the decoder. B–D: the three inputs of Reg 1.
- E–F: selectors below the two read multiplexers.
- Right-click each BLANK tunnel; edit Net Name, then save.

Q2: Understand the supplied write control



- For i = 1…31: enable[i] = RegWrite AND (WriteReg == i).
- Here, RegWrite = 1 passes WriteReg to the decoder.
- RegWrite = 0 forces decoder address 0; output 0 is unused.
- Read 0 is a 32-bit constant zero, with no writable storage.
- Question: why would RegWrite alone enable too much?

Q2: Understand the supplied write control



- For i = 1…31: enable[i] = RegWrite AND (WriteReg == i).
- Here, RegWrite = 1 passes WriteReg to the decoder.
- RegWrite = 0 forces decoder address 0; output 0 is unused.
- Read 0 is a 32-bit constant zero, with no writable storage.
- Question: why would RegWrite alone enable too much?

RegWrite alone would update every register.
Writes to x0 enable to no storage.

Q3: Predict before you test

- Finish the worksheet table in order; then test your predictions.

Test, explain, repair

- Save; run the green Register File Test block’s test cases.
- Unconnected input? Check that all six tunnel names are filled.
- Unexpected value? Identify the read selector and last valid write.
- Check RegWrite, destination, and the clock edge together.
- Keep expected outputs unchanged; explain a failure before editing.

Q4: Discuss



From this circuit to your RISC-V CPU (lab 4)



- rs1 / rs2 → ReadReg1 / ReadReg2; rd → WriteReg.
- Writeback result → WriteData; control → RegWrite; CPU clock → Clock.
- ReadData1 / ReadData2 supply register operands to the datapath.
- Can two ports read the same register at once? Why?
- If one instruction reads while another writes, which value is needed?