

Question 1: From Devices to Abstractions Put the following levels in order from **lowest-level physical device** to **highest-level computational abstraction**:

transistor logic gate ALU RISC-V instruction

Briefly explain why computer architects use these layers of abstraction rather than reasoning about every transistor individually.

Question 2: Transistors T/F 2.1. A pMOS transistor behaves as a closed switch when V_g is high.

- ☐ True
☐ False

2.2. nMOS transistors are part of the pull-up network.

- ☐ True
☐ False

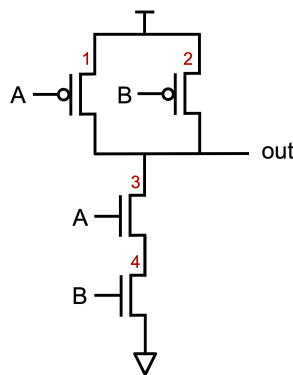
2.3. An nMOS transistor behaves as an open switch when V_g is high.

- ☐ True
☐ False

2.4. In an nMOS transistor, current can flow between source and drain when V_g is low.

- ☐ True
☐ False

Question 3: CMOS Gates Use the transistor diagram below to answer the following questions. Each transistor is numbered in order to make answering the following questions more clear.



3.1. Which transistors are on when $A = 0$ and $B = 0$?

- ☐ 1

- ☐ 2
- ☐ 3
- ☐ 4

3.2. What is the output when $A = 0$ and $B = 0$?

3.3. Which network is driving the output when $A = 0$ and $B = 0$?

- ☐ Pull-up
- ☐ Pull-down

3.4. Which transistors are on when $A = 1$ and $B = 0$?

- ☐ 1
- ☐ 2
- ☐ 3
- ☐ 4

3.5. What is the output when $A = 1$ and $B = 0$?

3.6. Which network is driving the output when $A = 1$ and $B = 0$?

- ☐ Pull-up
- ☐ Pull-down

3.7. Which transistors are on when $A = 1$ and $B = 1$?

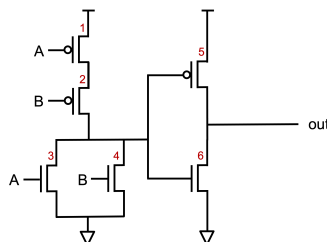
- ☐ 1
- ☐ 2
- ☐ 3
- ☐ 4

3.8. What is the output when $A = 1$ and $B = 1$?

3.9. Which network is driving the output when $A = 1$ and $B = 1$?

- ☐ Pull-up
- ☐ Pull-down

Question 4: More CMOS Use the transistor diagram below to answer the following questions. Each transistor is numbered in order to make answering the following questions more clear.



4.1. Which transistors are on when $A = 0$ and $B = 0$?

- ☐ 1
- ☐ 2
- ☐ 3
- ☐ 4
- ☐ 5
- ☐ 6

4.2. What is the output when $A = 0$ and $B = 0$?

4.3. Which network is driving the output when $A = 0$ and $B = 0$?

- ☐ Pull-up
- ☐ Pull-down

4.4. Which transistors are on when $A = 1$ and $B = 0$?

- ☐ 1
- ☐ 2
- ☐ 3
- ☐ 4
- ☐ 5
- ☐ 6

4.5. What is the output when $A = 1$ and $B = 0$?

4.6. Which network is driving the output when $A = 1$ and $B = 0$?

- ☐ Pull-up
- ☐ Pull-down

Question 5: Equation to Truth Tables Fill in the truth table for the following equations:

$ABC + \overline{A}B\overline{D}$					$\overline{A + B + C} + D$				
A	B	C	D	Y	A	B	C	D	Y
0	0	0	0	_____	0	0	0	0	_____
0	0	0	1	_____	0	0	0	1	_____
0	0	1	0	_____	0	0	1	0	_____
0	0	1	1	_____	0	0	1	1	_____
0	1	0	0	_____	0	1	0	0	_____
0	1	0	1	_____	0	1	0	1	_____
0	1	1	0	_____	0	1	1	0	_____
0	1	1	1	_____	0	1	1	1	_____
1	0	0	0	_____	1	0	0	0	_____
1	0	0	1	_____	1	0	0	1	_____
1	0	1	0	_____	1	0	1	0	_____
1	0	1	1	_____	1	0	1	1	_____
1	1	0	0	_____	1	1	0	0	_____
1	1	0	1	_____	1	1	0	1	_____
1	1	1	0	_____	1	1	1	0	_____
1	1	1	1	_____	1	1	1	1	_____

Question 6: Truth Table to Boolean Diagram What Boolean equation corresponds to this truth table?

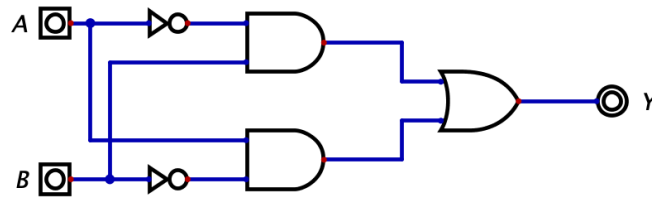
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Question 7: XOR Which of the following equations is logically equivalent to $A \oplus B$?

- ☐ $AB + \overline{A} \cdot \overline{B}$
- ☐ $AB + \overline{A}\overline{B}$
- ☐ $\overline{A}\overline{B} + \overline{A}B + A\overline{B}$
- ☐ $A\overline{B} + \overline{A}B$
- ☐ $AB + \overline{A}B + A\overline{B}$

Question 8: 3-input Gates If it takes 6 transistors to make a 3-input NAND gate, how many transistors does it take to make a 3-input AND gate?

Question 9: Transistor Counting How many transistors are in the below circuit?



Question 10: DeMorgan's Practice Simplify the following expressions using DeMorgan's law. Make sure your final solution is in Sum Of Products form.

10.1. $\overline{AB + CD}$

10.2. $\overline{(A + B)(C + D)EF}$

10.3. $\overline{\overline{A + B\overline{C}} + D(\overline{D\overline{F}})}$

10.4. $\overline{AB + \overline{CD} + \overline{FG}}$

Question 11: Boolean Algebra Simplify the following boolean equations.

11.1. $(AB + AC)AD + C$

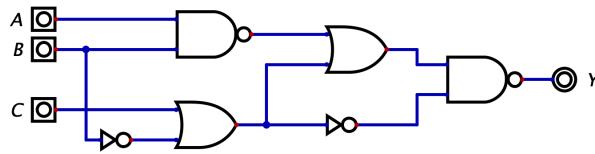
11.2. $\overline{\overline{A}} \cdot \overline{\overline{B}} + \overline{\overline{AB}} + \overline{\overline{C}} + (B + C)D$

11.3. $A(AB + \overline{BC})$

11.4. $\overline{(A+B)(C+D+E)} + \overline{(A+B)}$

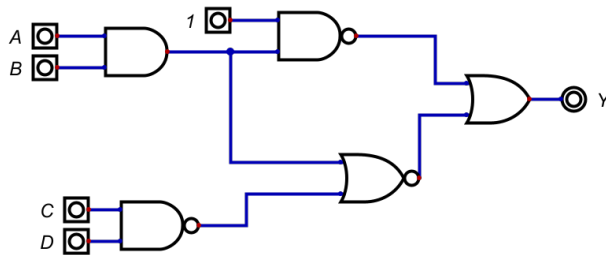


Question 12: Diagram to Equation Which of the following is the most simplified boolean equation representation of this gate diagram?



12.1.

- ☐ $Y = A + B + \overline{C}$
- ☐ $Y = AB + C + \overline{B}$
- ☐ $Y = A + \overline{B} + C$
- ☐ $Y = \overline{A} + \overline{B} + C$



12.2.

- ☐ $Y = \overline{D} + \overline{A} + \overline{C} + B$
- ☐ $Y = AC + BC + \overline{DA}$
- ☐ $Y = \overline{A} + \overline{B} + CD$
- ☐ $Y = \overline{AD(C+B)}$
- ☐ $Y = \overline{A} + \overline{B}$
- ☐ $Y = 1$

Question 13: Circuit Design We want to design a circuit that will output 1 when at least 2 out of the 3 inputs are 1 and 0 otherwise.

13.1. Fill in the truth table.

A	B	C	Y
0	0	0	_____
0	0	1	_____
0	1	0	_____
0	1	1	_____
1	0	0	_____
1	0	1	_____
1	1	0	_____
1	1	1	_____

13.2. Which of the following equations represent this truth table?

- ☐ $AB + AC + BC$
- ☐ $AB + BC$
- ☐ $A + B + C$
- ☐ $AB + BC + AC + ABC$

13.3. Now, we want to simplify this function in order to reduce the transistor count of our final design. Find the simplified SOP form of this equation.

13.4. Draw the circuit diagram for the equation.