COMP311 Extra Practice 1 Name: _____

Question 1: Boolean Algebra Simplify the following Boolean expression, and express the result in terms of SOP form.

1.1. $\overline{AB} \oplus C + A + CB$

1.2. $\overline{\bar{A} + \bar{B}} + \overline{AB}(C + \bar{C}(D + \overline{D + \bar{E}}))$

Question 2: Reducing Transistors Explain in a couple sentence why we need to care about transistor counts when designing circuits? What strategies can we use to reduce transistor counts?

Question 3: Problem 1: Two-Bit Comparator *(Very similar to the comparator example from class slides.)*

Let $A = A_1A_0$ and $B = B_1B_0$ be two-bit unsigned numbers.

Define an output Y such that:

$$Y = 1 \iff A > B + 1$$

3.1. Construct the truth table for Y.

3.2. Write the Sum-of-Products (SOP) expression for Y.

3.3. Derive the simplest Boolean expression for Y.

Question 4: Problem 2: Transistor Count Optimization (NOR-only) Assume CMOS gates with the following transistor counts:

Gate	Transistors
NOT	2
NAND (2-input)	4
NOR (2-input)	4
AND (2-input)	6
OR (2-input)	6

Given the Boolean function:

$$F = (A + B)(\bar{C} + D)$$

4.1. Implement F using AND, OR, and NOT gates. Count the total number of transistors.

4.2. Rewrite F using **only NOR gates and inverters**.

4.3. Compute the new transistor count and determine which implementation is cheaper.

Question 5: Problem 3: Boolean Reduction Simplify the following Boolean expression as much as possible:

$$F = A\bar{B} + AB + A\bar{B}C$$

Show each step and clearly state the Boolean laws used.

Question 6: Problem 4: Universal Gates 6.1. Which two logic gates are universal?

6.2. Explain why a gate being universal is useful.

6.3. Give one advantage and one disadvantage of using only universal gates in a circuit.

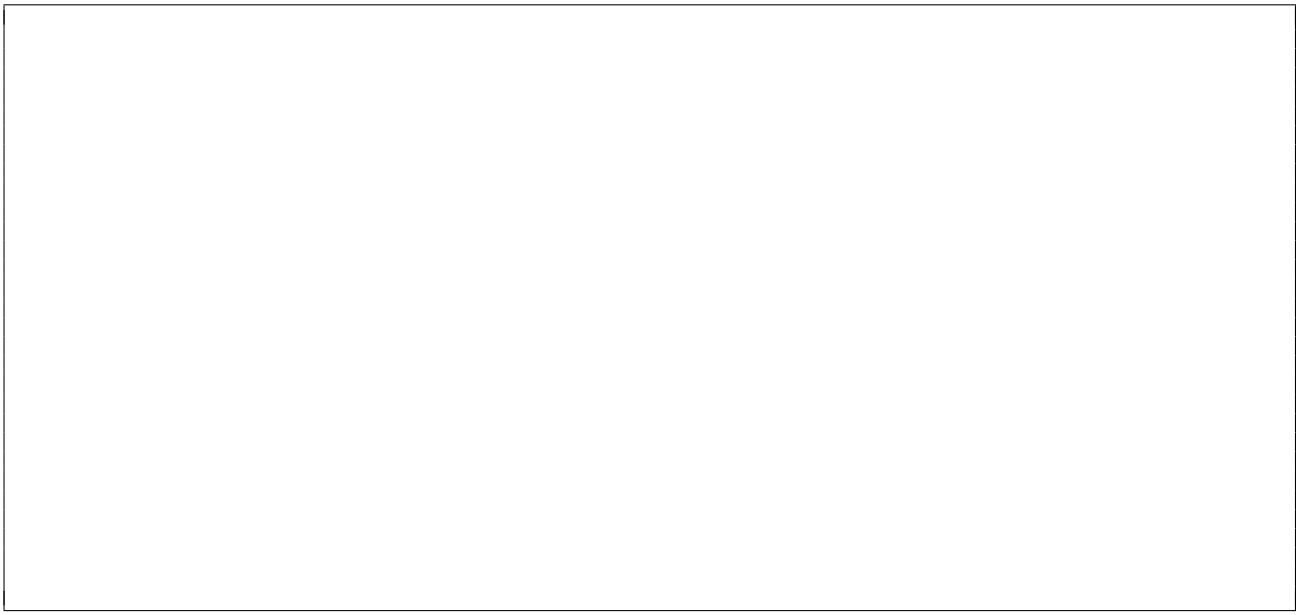
Question 7: Problem 1 Simplify:

$$\overline{\left(A + \overline{A}B + \overline{AB}\right)} + \overline{\left(A + \overline{B}\right)}$$

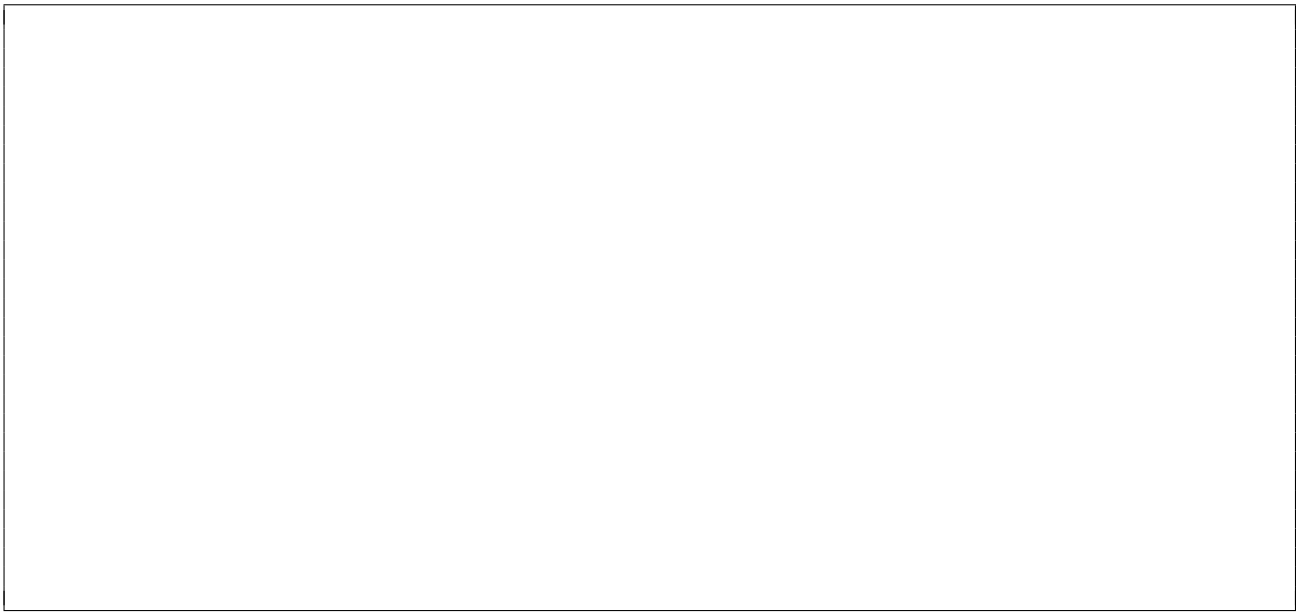
Question 8: Problem 2 Simplify:

$$\overline{AB} + \overline{A}B\overline{C} + \overline{\left(A + \overline{C}\right)}$$

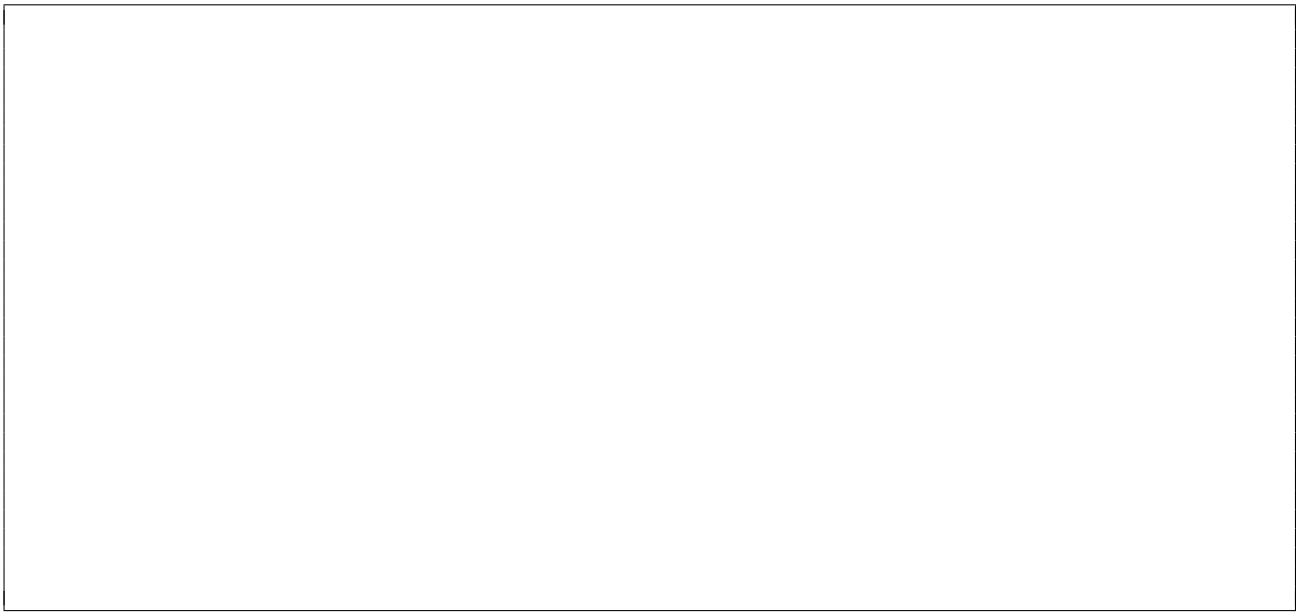
Question 9: 8:1 Mux Design Design an 8:1 mux using only 2:1 muxes



Question 10: XOR Gate Design Implement a two input XOR gate using a 4:1 mux



Question 11: 4:1 Mux Design Design a 4:1 mux using logic gates



Question 12: Transistor Minimization Minimize the transistor count for your 4:1 mux