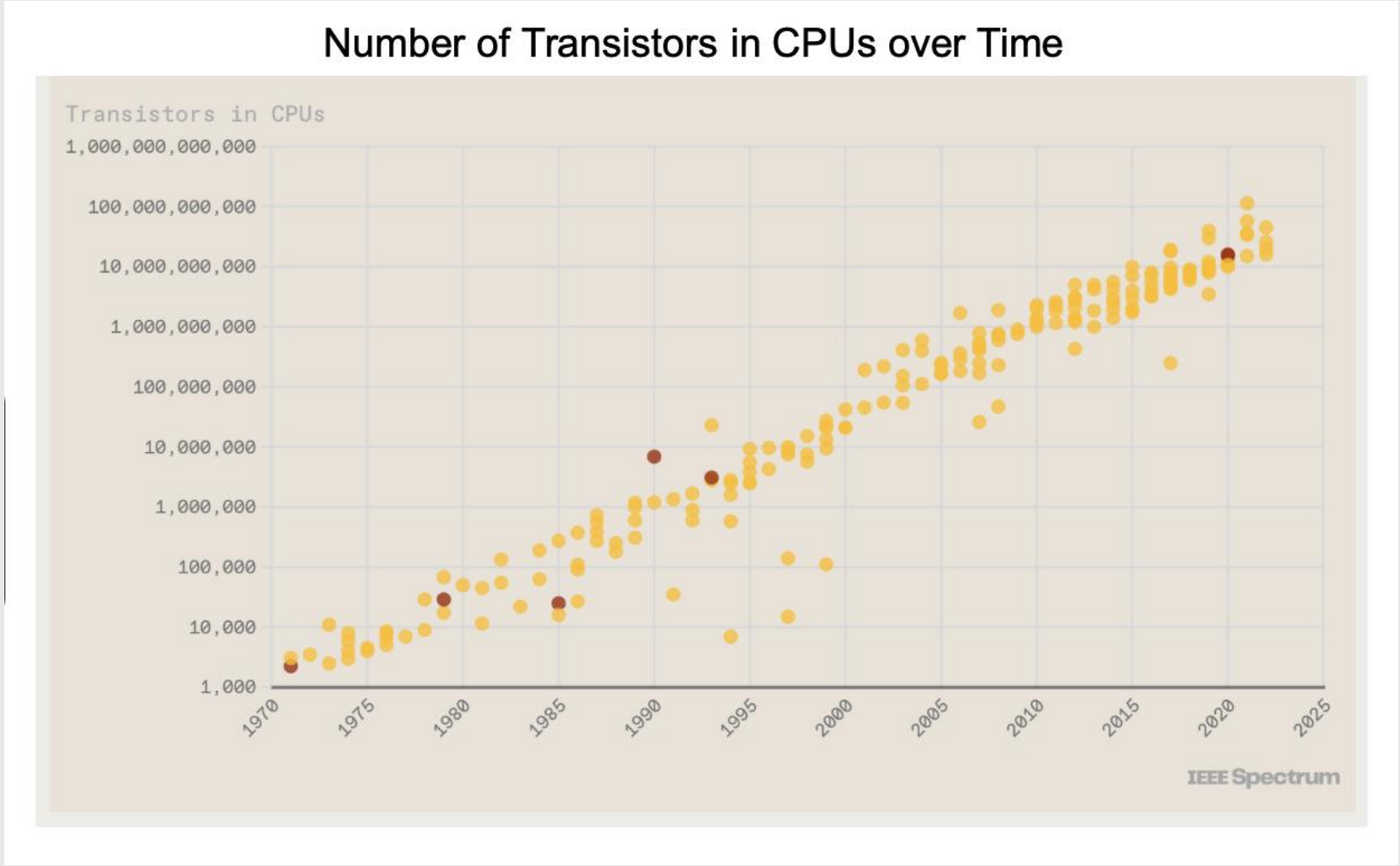
COMP311: *COMPUTER ORGANIZATION!*

Lecture 4: Transistors, Intro to CMOS Gates

tinyurl.com/comp311-sp26

TRANSISTORS

Transistors are the physical building blocks of modern computers!



A transistor is the physical device we use to turn continuous electrical behavior into digital 0s and 1s.

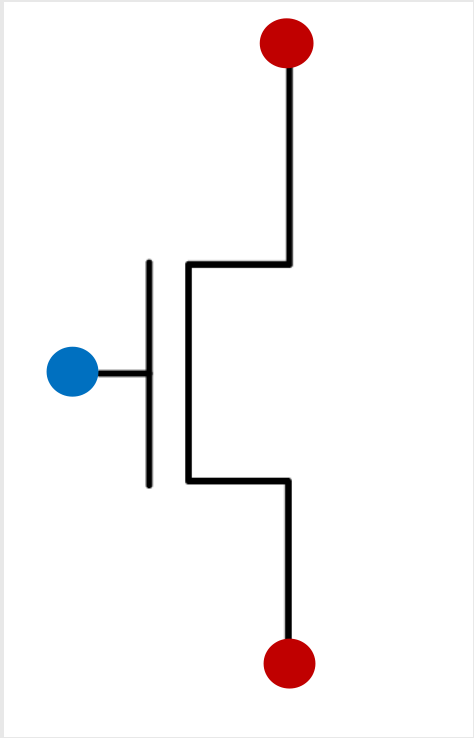
You can think of it as an electrically controlled switch that turns current on or off.

Transistors

- We will be working with two types of transistors
  - *nMOS transistors*
  - *pMOS transistors*
- There are three terminals
  - *Gate: controls whether the transistor is on or off*
  - *Source and Drain: endpoints*

Transistor Symbol

Switch

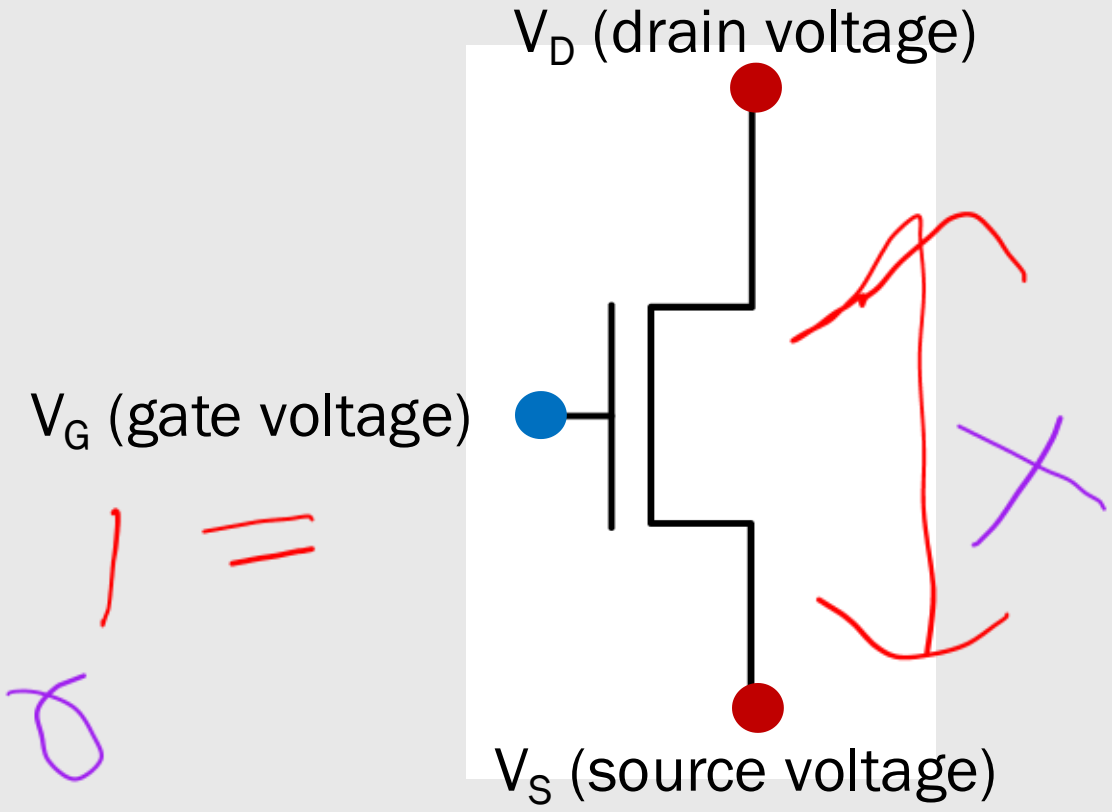


Transistor
(n-channel MOSFET)

The terminal labeled with the blue dot determines whether current can flow between the terminals labeled with the red dot.

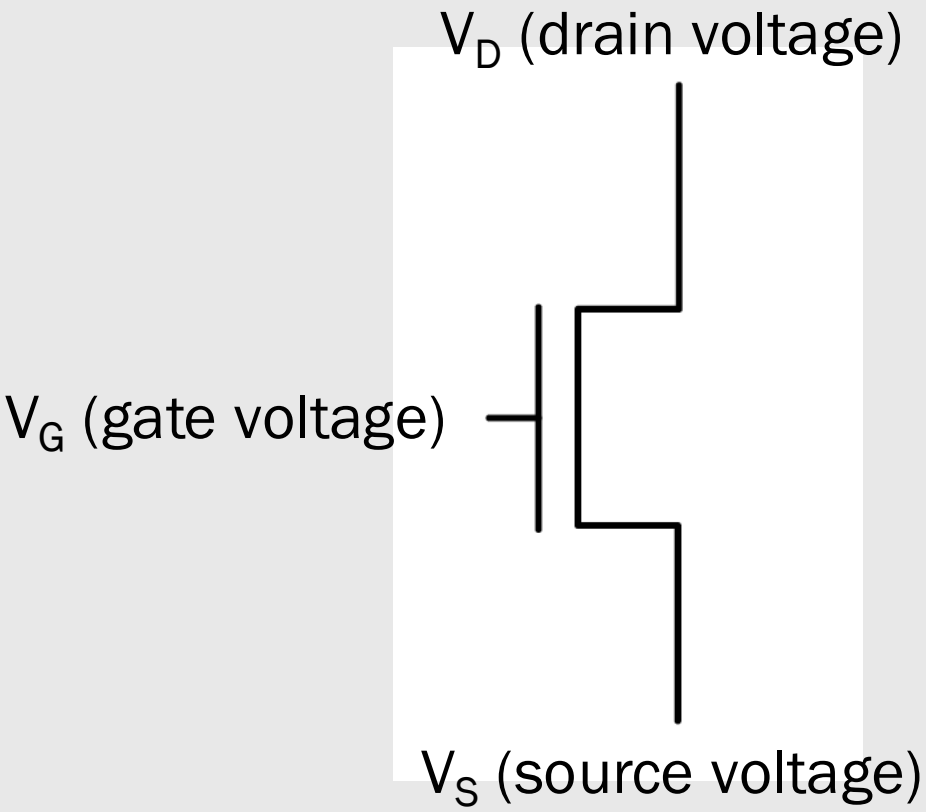
NMOS Transistor

- There are three terminals
  - *Gate: controls whether the transistor is on or off*
  - *Source and Drain: endpoints*



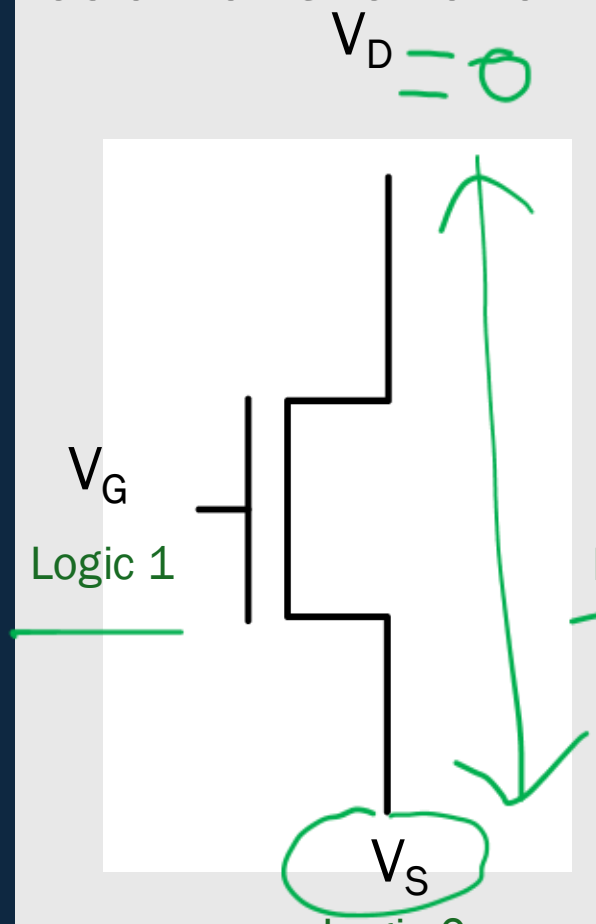
NMOS Transistor

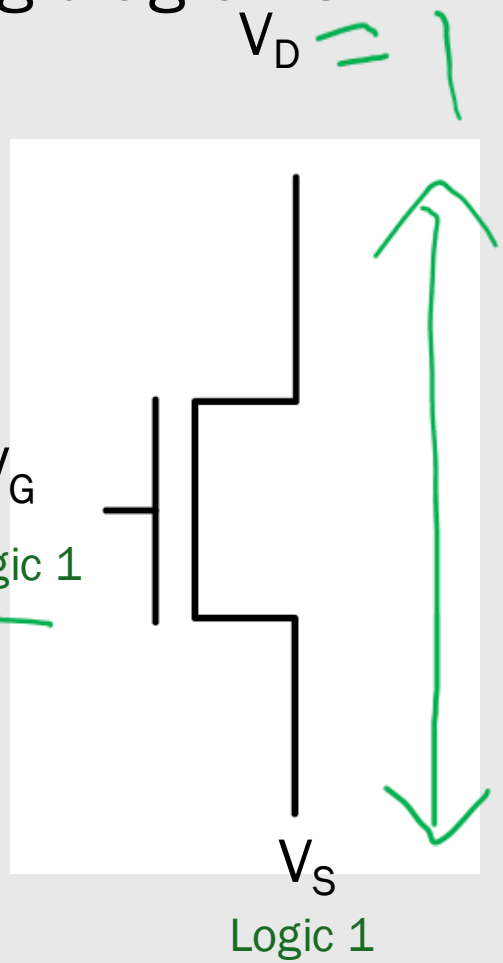
- If the gate voltage is high (logic 1), current can flow between source and drain
  - *The source and drain will be connected and will have the same voltage*
- If the gate voltage is low, current cannot flow between source and drain
  - *The source and drain are not connected*

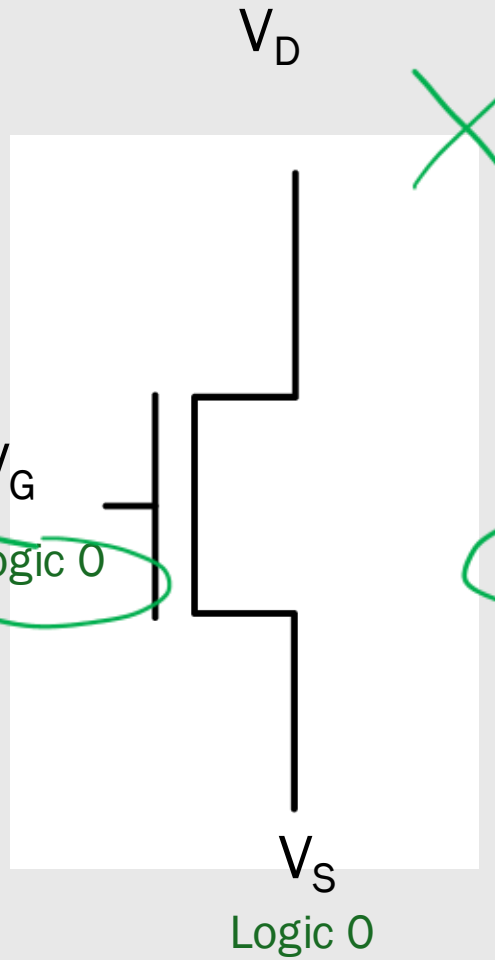


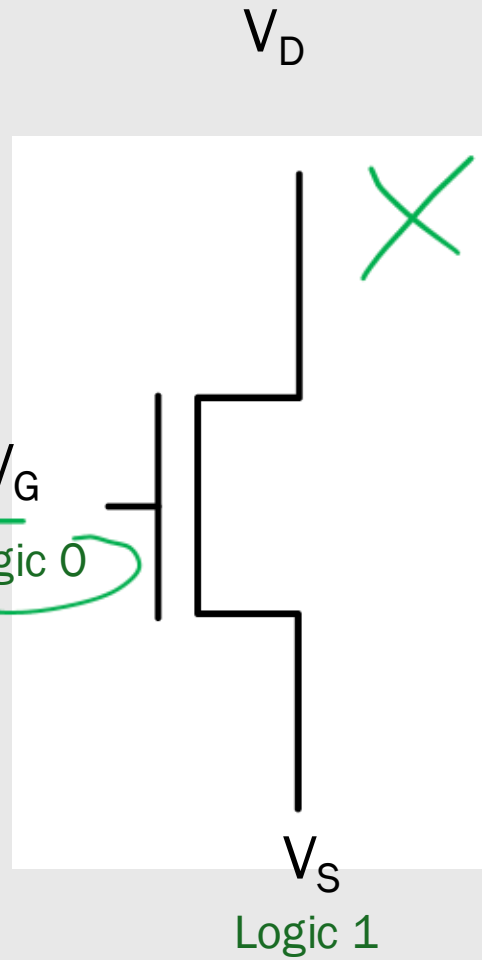
NMOS Transistor

Let's say that we know the values of V_G and V_S. What is the value of V_D in each of the following diagrams?

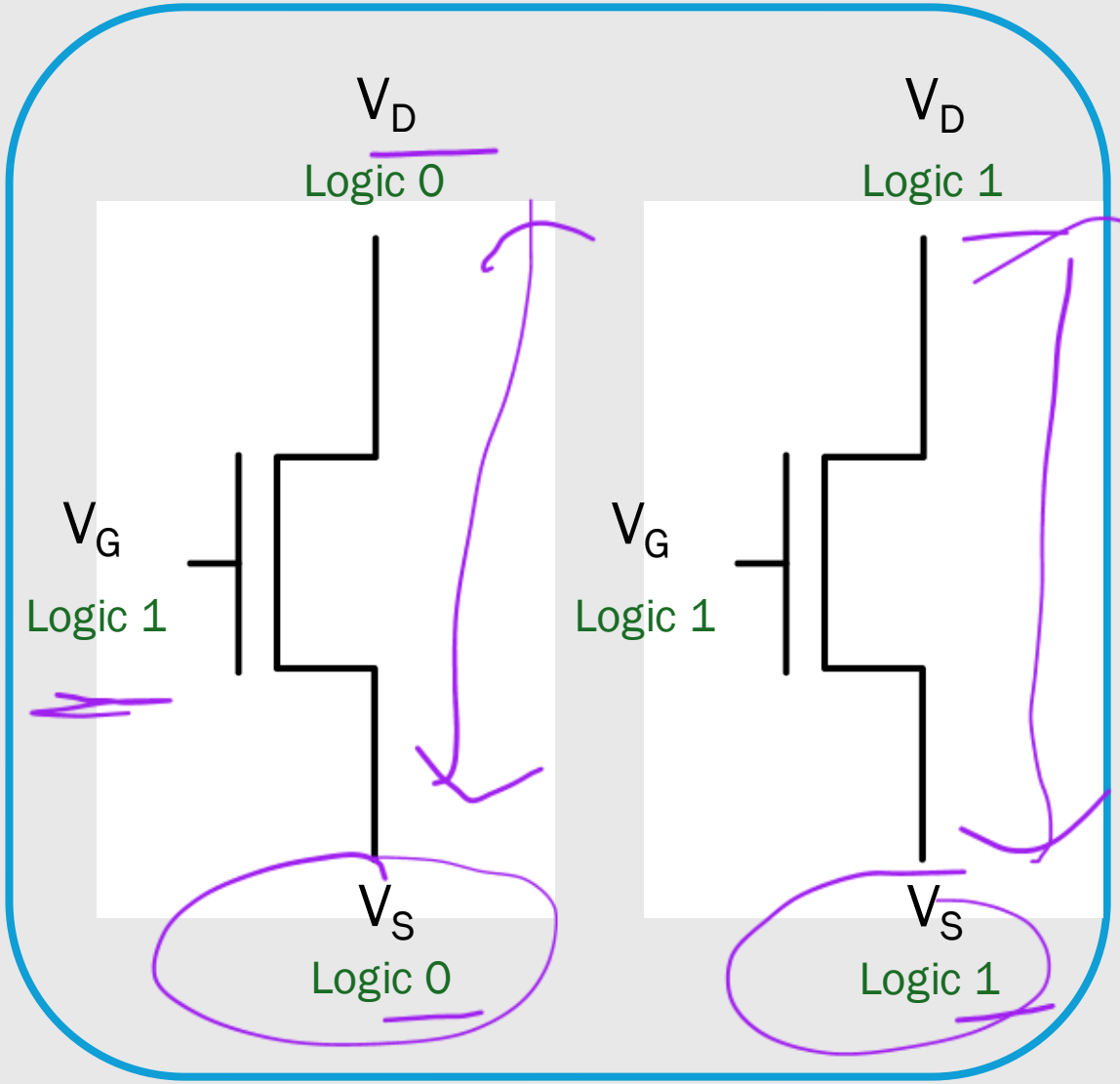




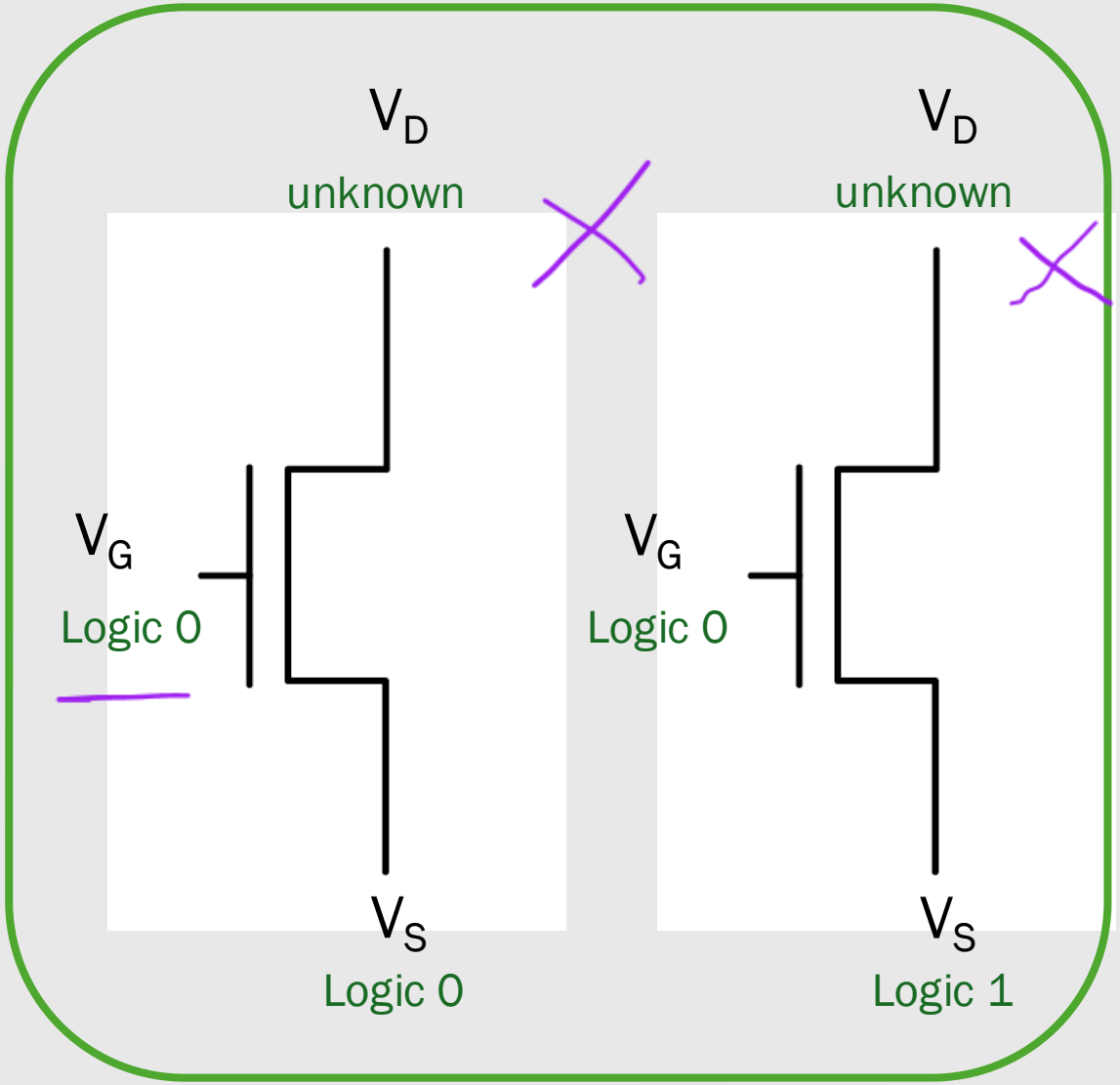




NMOS Transistor



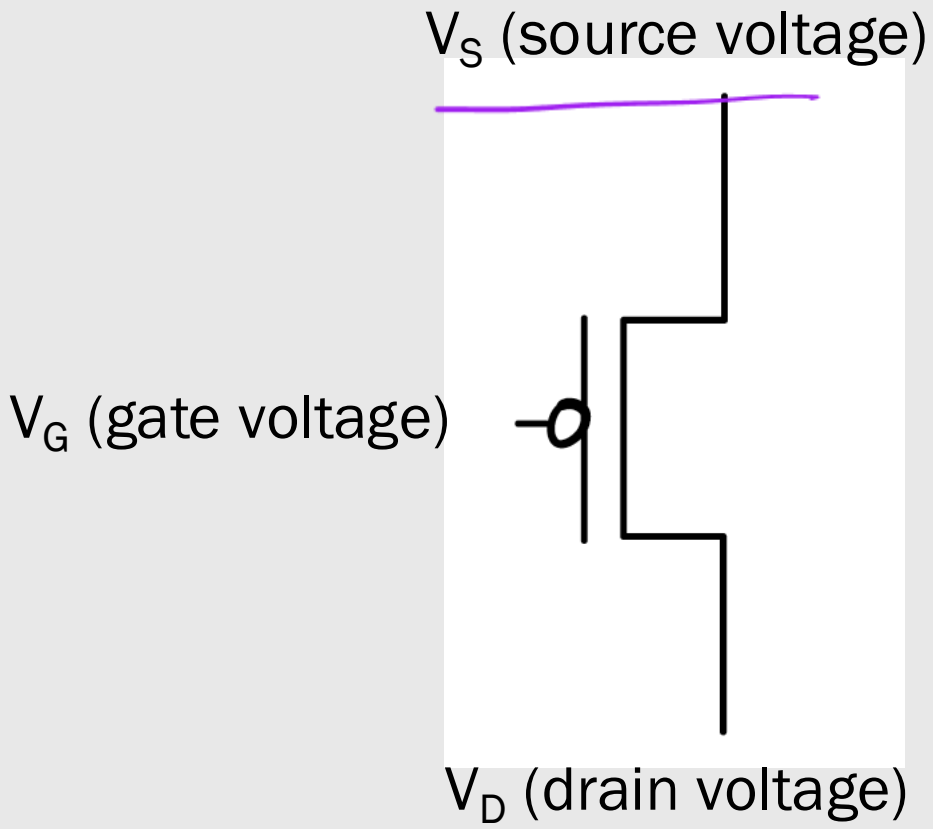
V_G is high, so source and drain are connected



V_G is low, so source and drain are not connected

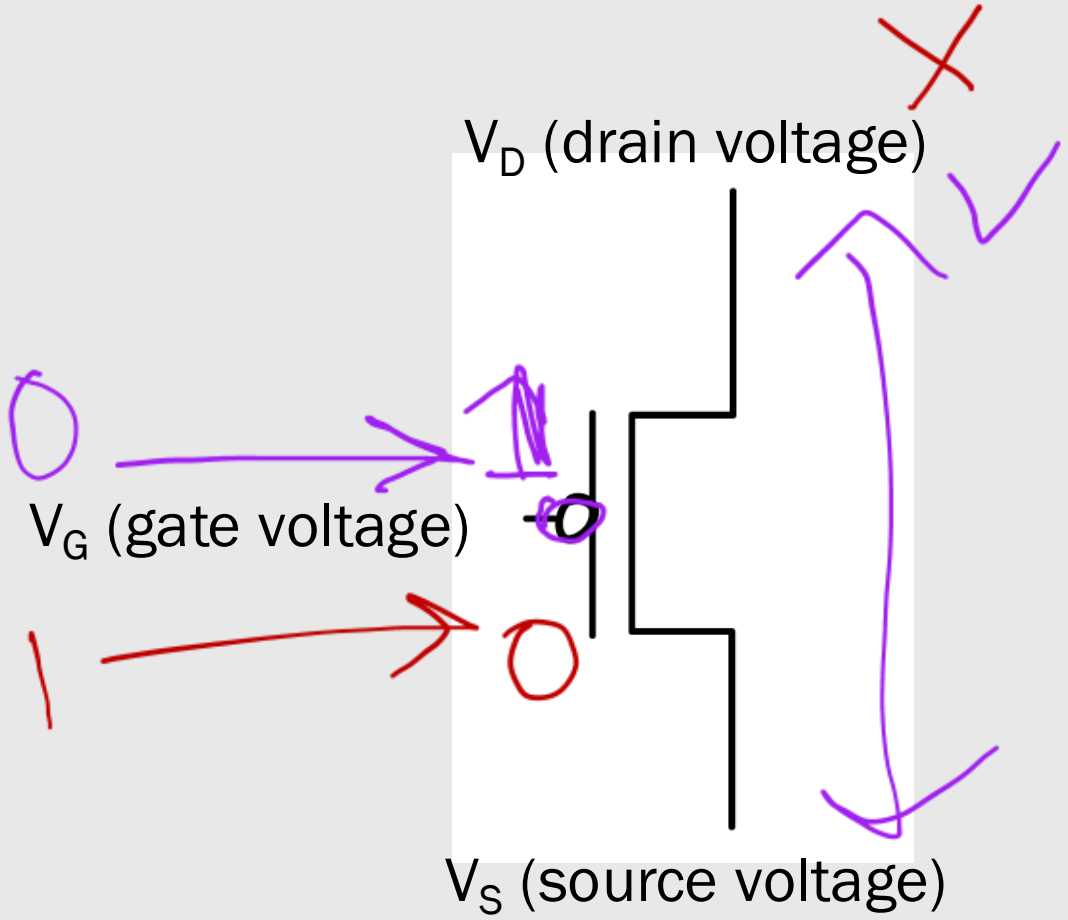
PMOS Transistor

- There are three terminals
  - *Gate: controls whether the transistor is on or off*
  - *Source and Drain: endpoints*



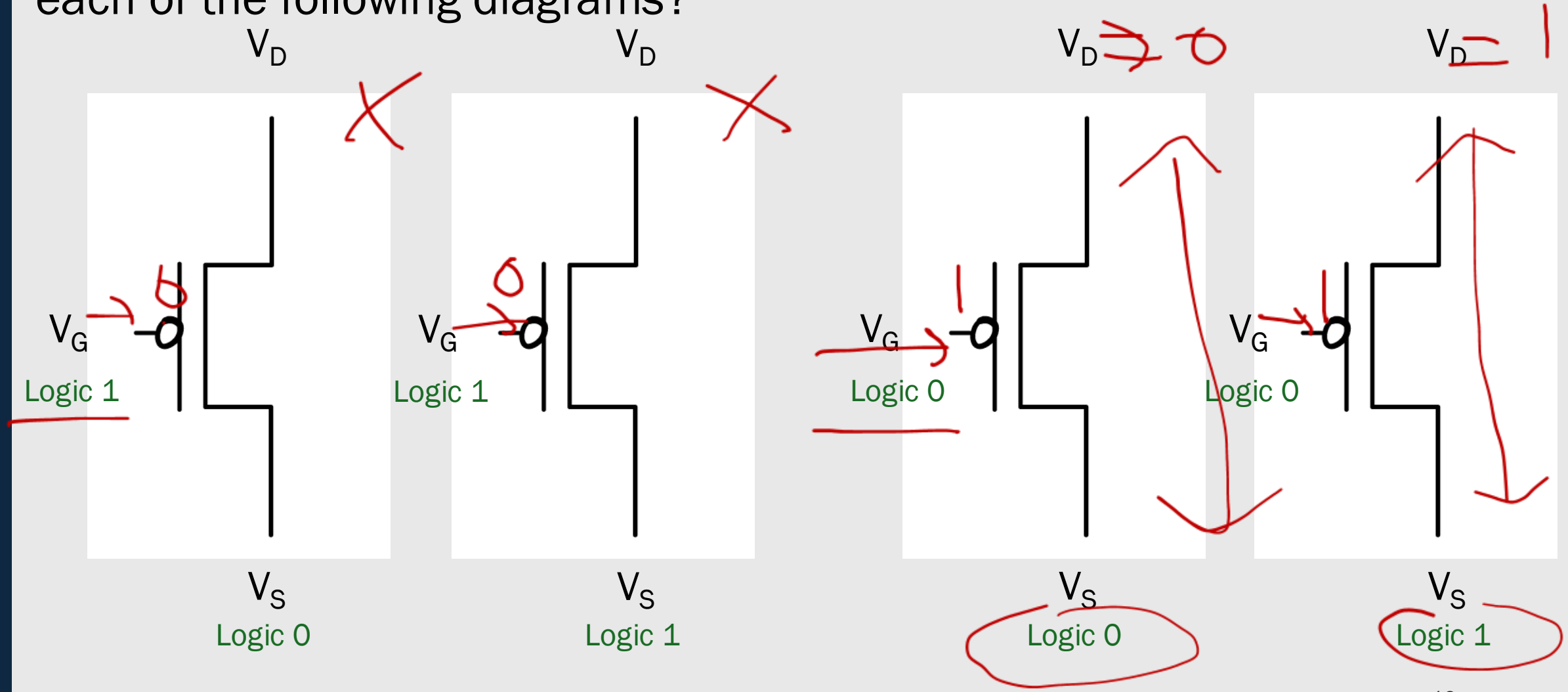
PMOS Transistor

- If the gate voltage is low (logic 0), current can flow between source and drain
  - *This source and drain will be connected and will have the same voltage*
- If the gate voltage is high, current cannot flow between source and drain
  - *The source and drain are not connected*

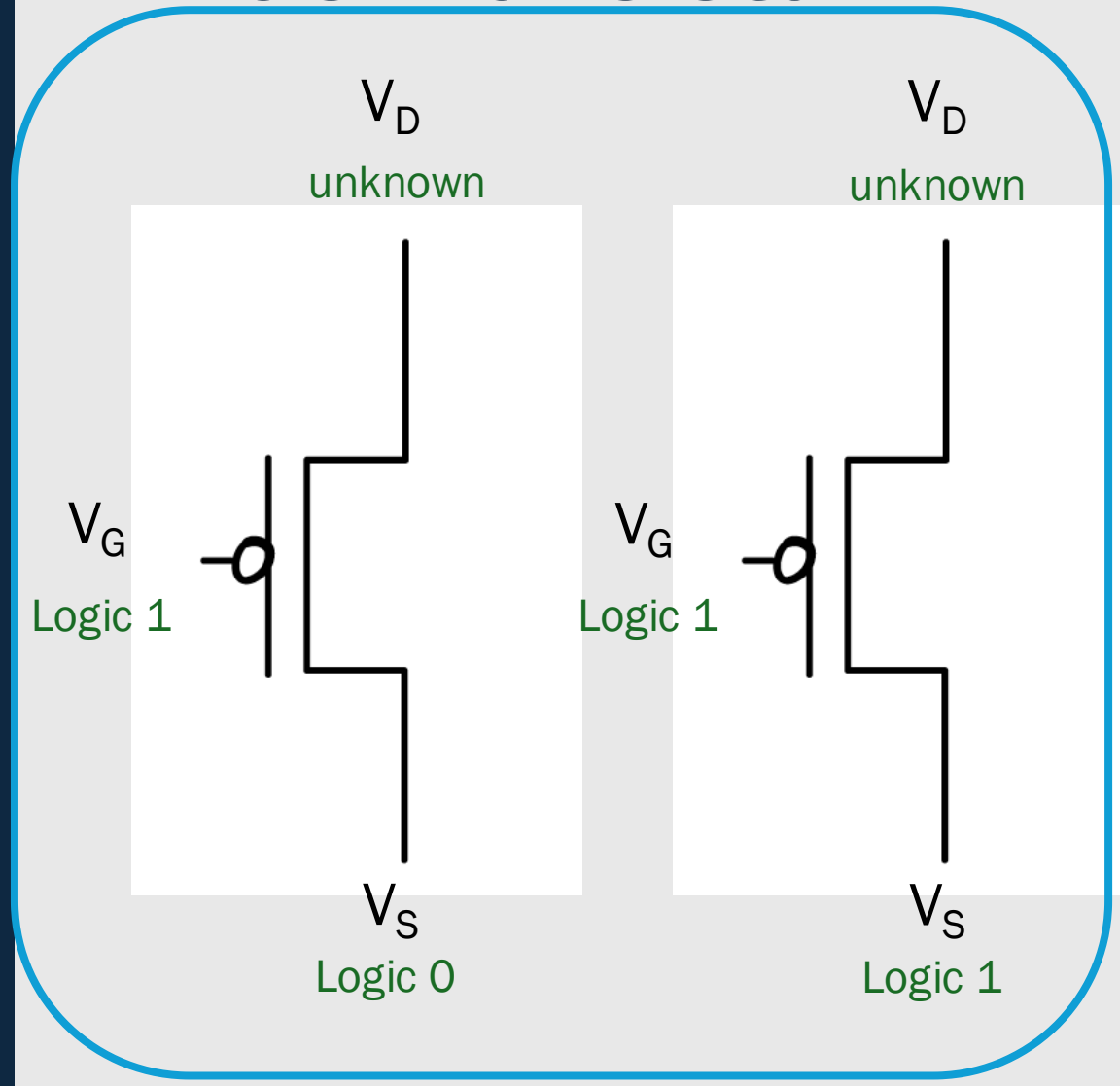


PMOS Transistor

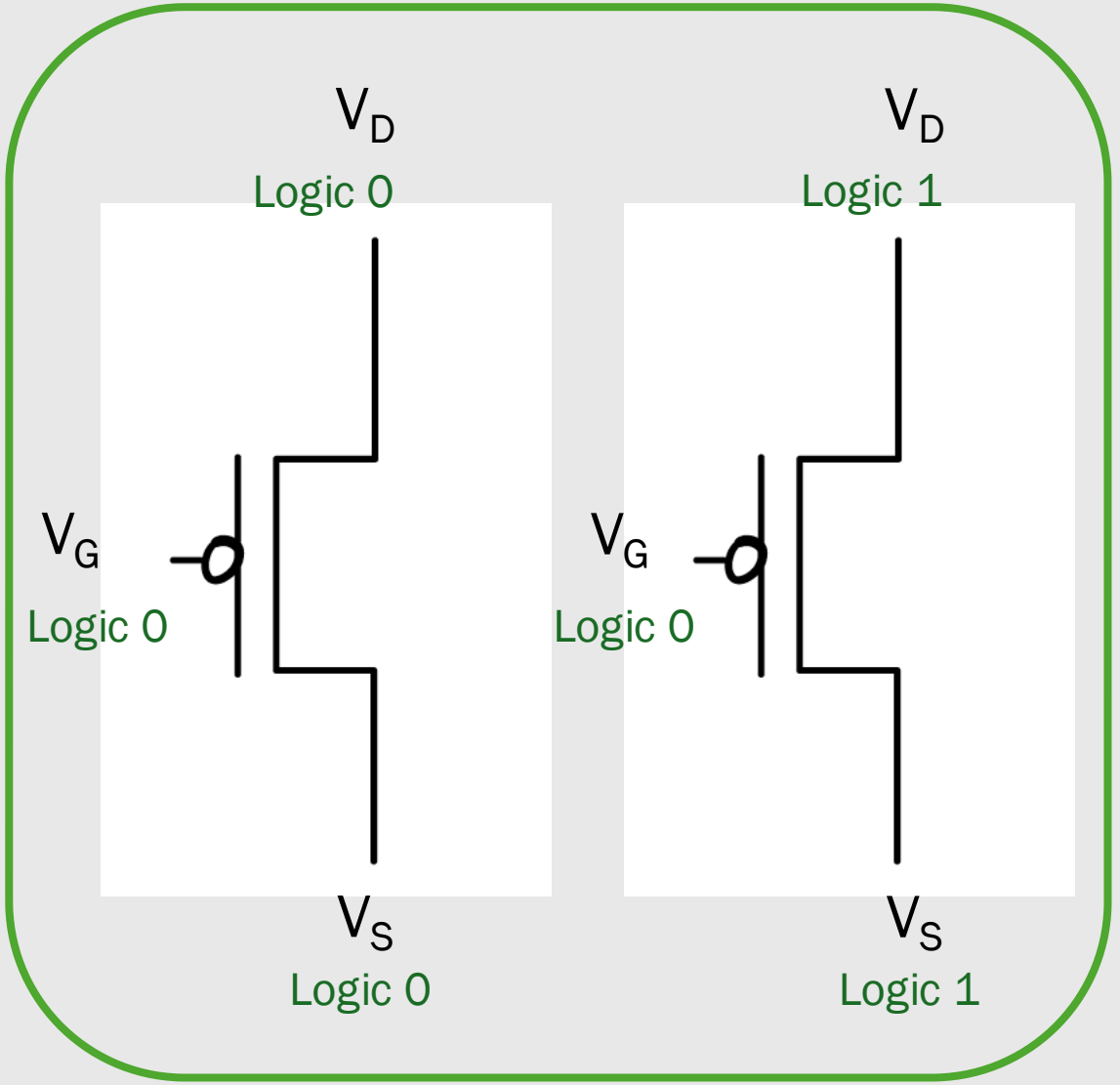
Let's say that we know the values of V_G and V_S. What is the value of V_D in each of the following diagrams?



PMOS Transistor

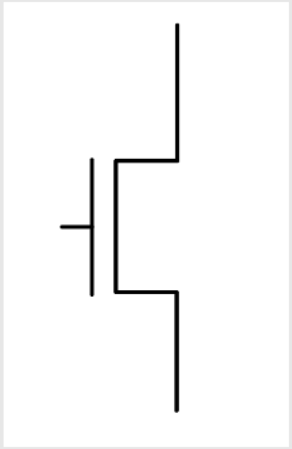
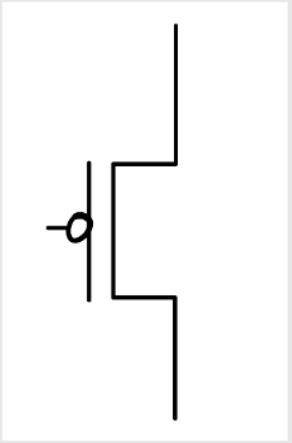


V_G is high, so source and drain are not connected

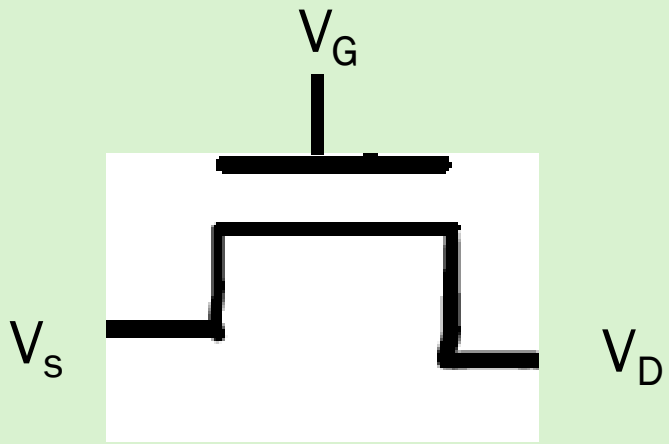


V_G is low, so source and drain are connected

Two Types of Transistors

	nMOS	pMOS
		
Behaves as an open switch when	Vg is low	Vg is high
Behaves as a closed switch when	Vg is high	Vg is low

nMOS Transistors



nMOS

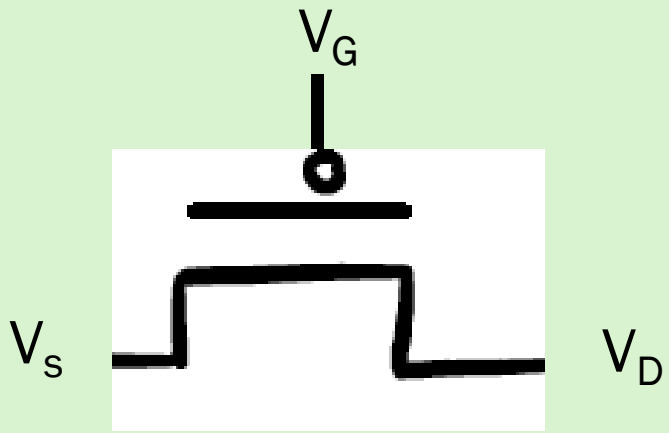
Acts as a(n) _____ (open/closed) switch when the gate voltage (Vg) is low.

Meaning that current _____ (can/cannot) flow between source and drain.

Acts as a(n) _____ (open/closed) switch when the gate voltage (Vg) is high.

Meaning that current _____ (can/cannot) flow between source and drain.

pMOS Transistors



pMOS

Acts as a(n) _____ (open/closed) switch when the gate voltage (Vg) is low.

Meaning that current _____ (can/cannot) flow between source and drain.

Acts as a(n) _____ (open/closed) switch when the gate voltage (Vg) is high.

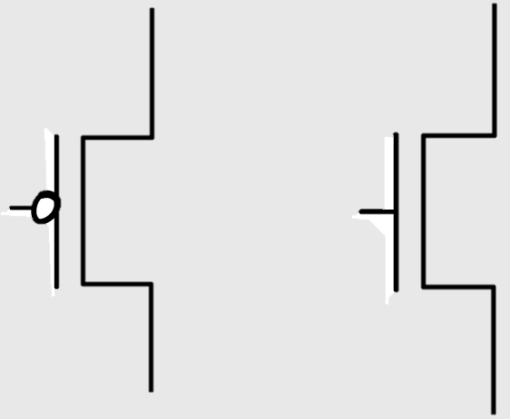
Meaning that current _____ (can/cannot) flow between source and drain.

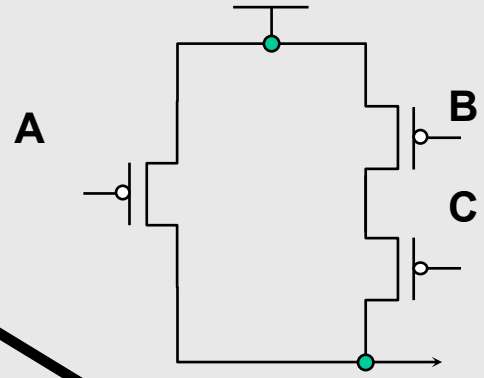
BUILDING LOGIC GATES WITH TRANSISTORS

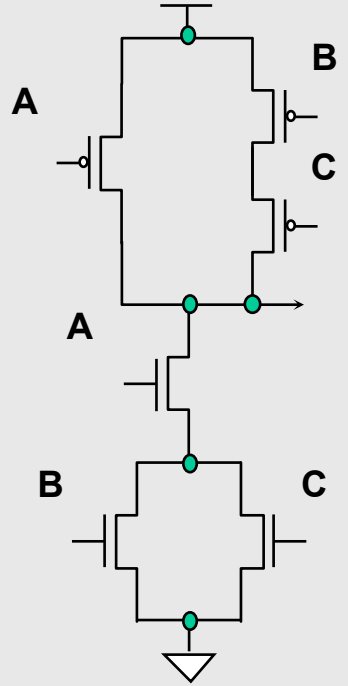
Abstraction ☺

CMOS Gates

Physical Transistors







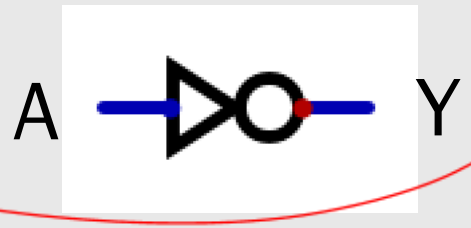
CMOS gates abstract away individual transistors, letting us design reliable logic at a higher level.

CMOS gates are the abstraction that lets many transistors behave like a single logical unit.

Let's Design an Inverter!

I want to design a circuit that takes as an input a one-bit value and outputs the complement of that number.

Symbol

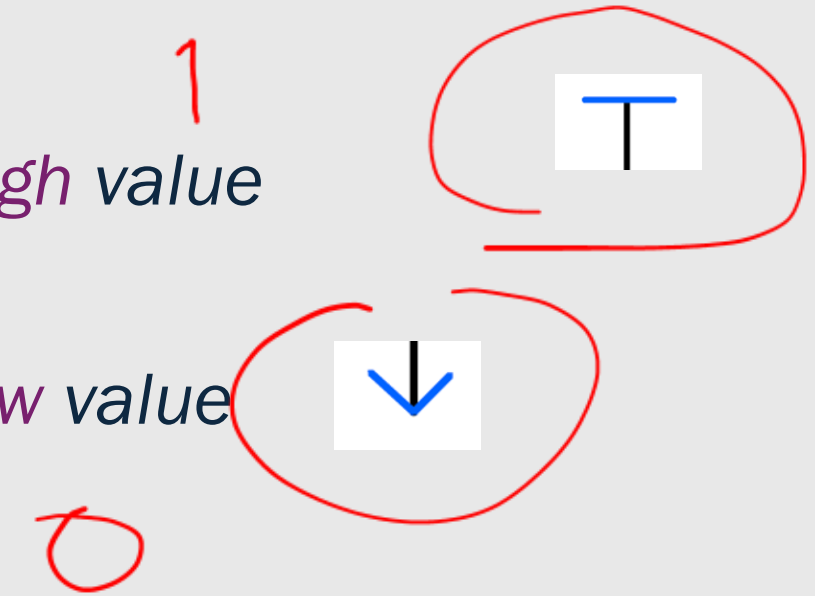


Truth Table

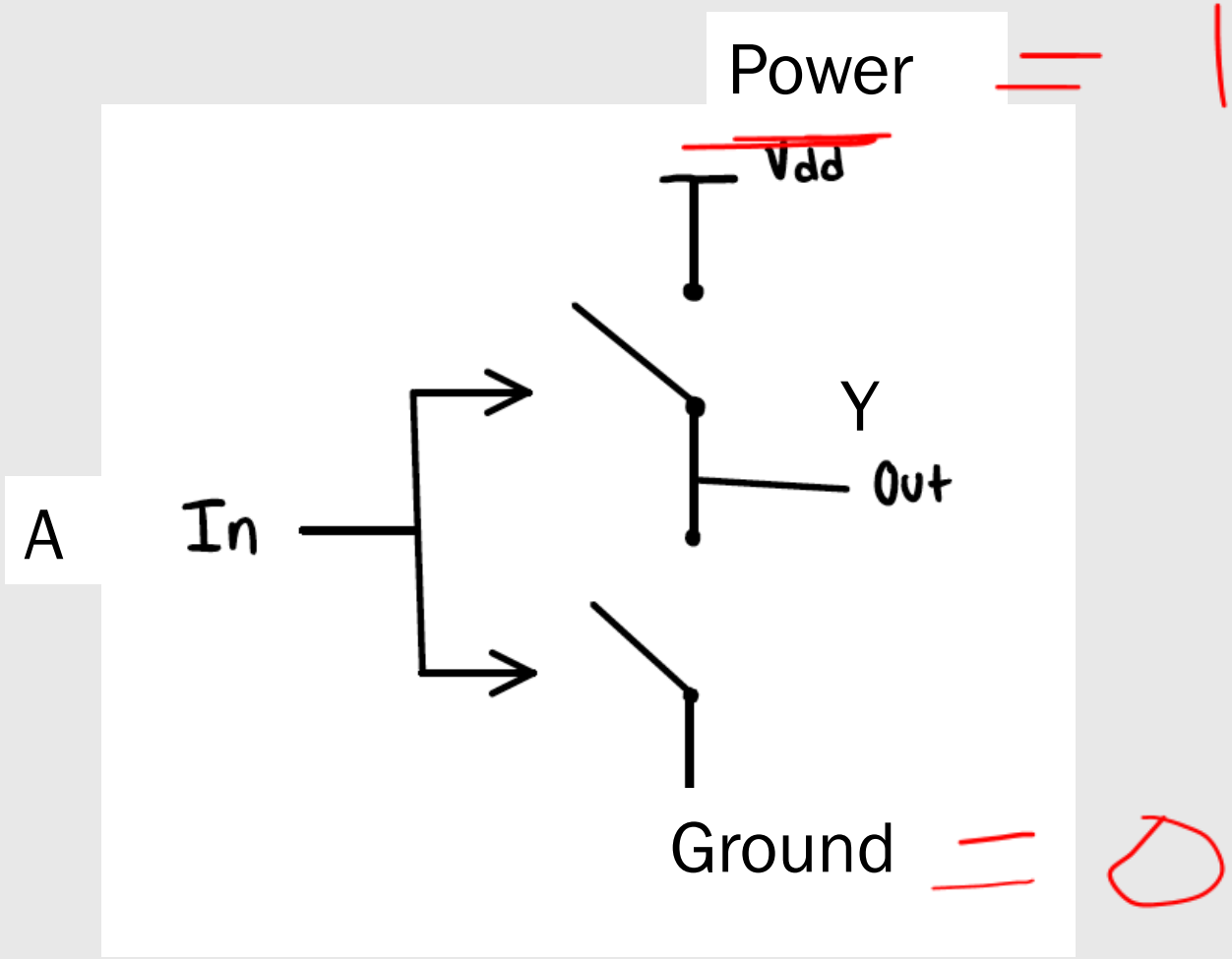
A	Y
0	1
1	0

New Components

- Power
  - *a component that produces a logic high value*
- Ground
  - *a component that produces a logic low value*

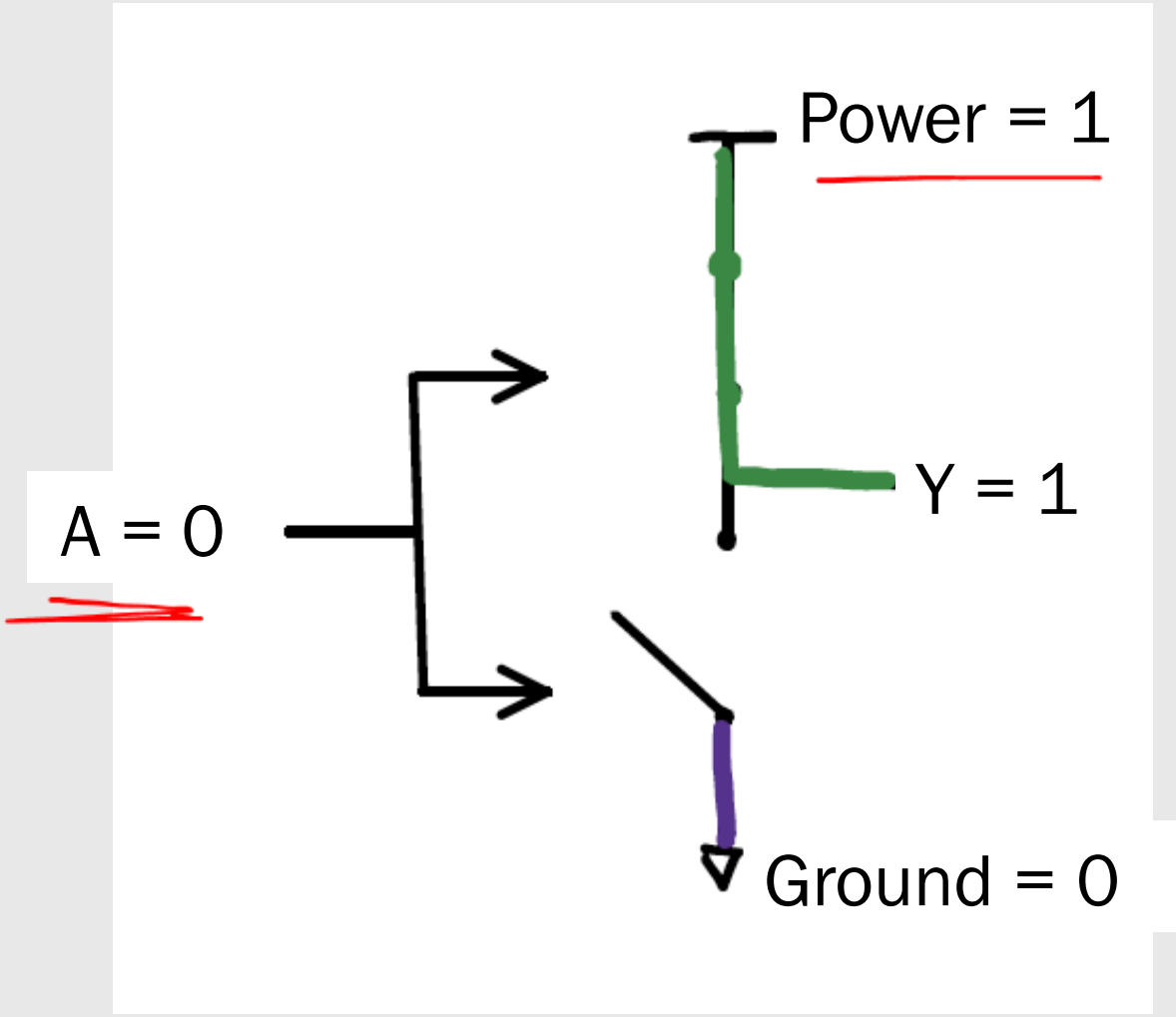


An Inverter with Switches



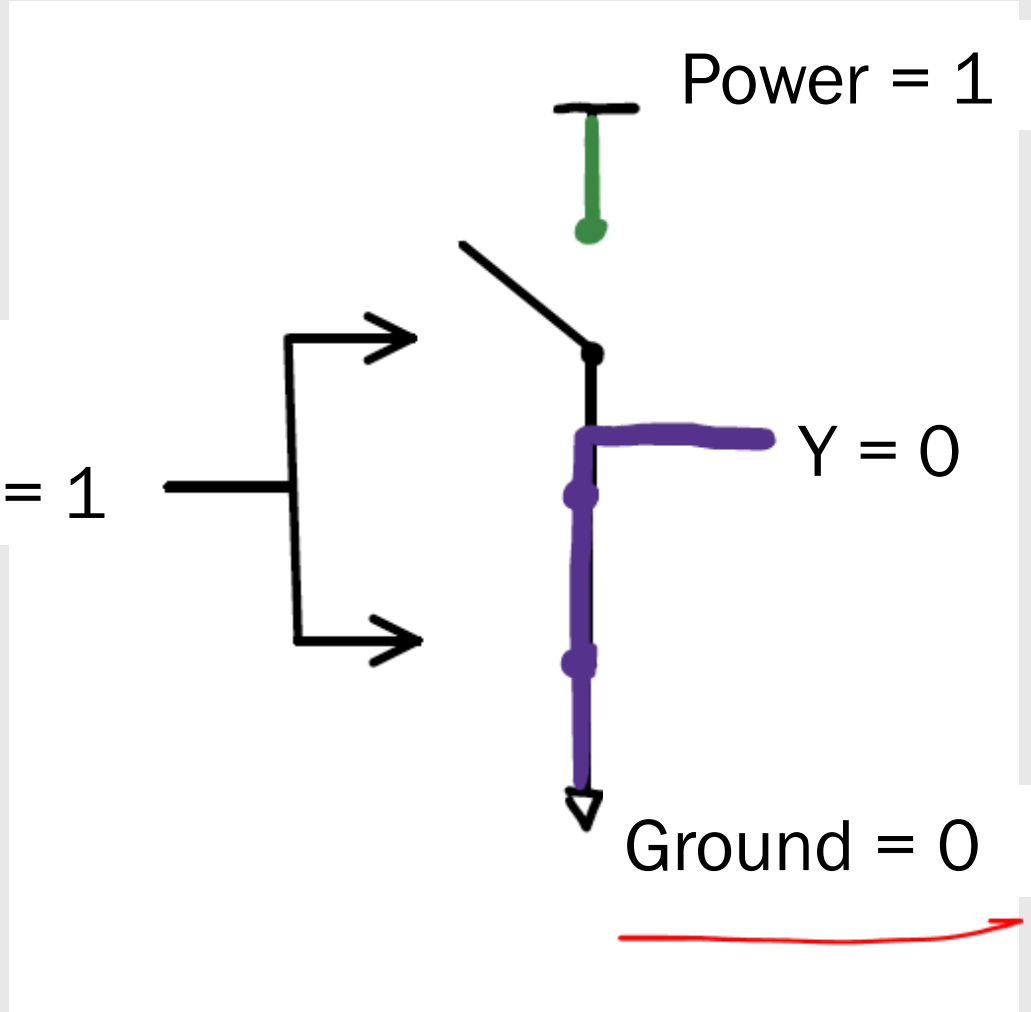
An Inverter with Switches

- When the input is 0
  - *The top switch is closed.*
  - *The bottom switch is open.*
  - *This will connect power to the output which will make the output 1.*



An Inverter with Switches

- When the input is 1
  - *The bottom switch is closed.*
  - *The top switch is open.*
  - *This will connect ground to the output which will make the output 0.*



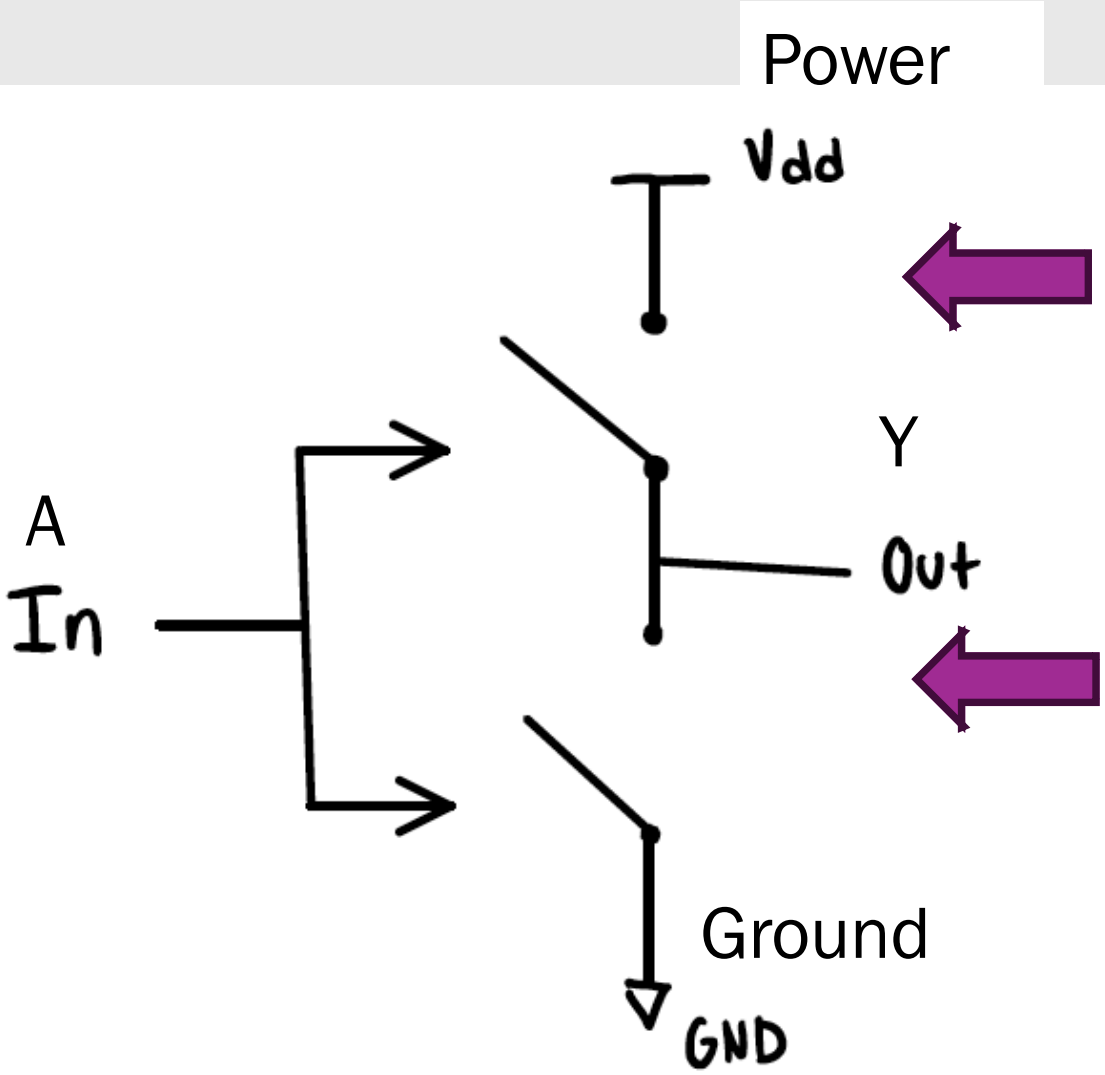
Building Logic Gates with Transistors

- Engineering Digital Behavior from Analog Devices
  - *NMOS transistors act as controllable connections to ground*
  - *PMOS transistors act as controllable connections to power*

CMOS gates work by carefully arranging these devices so physics is forced to produce clean digital logic!

Another way to say this: CMOS gates work by using NMOS transistors to pull outputs down and PMOS transistors to pull outputs up.

Building an Inverter with Transistors

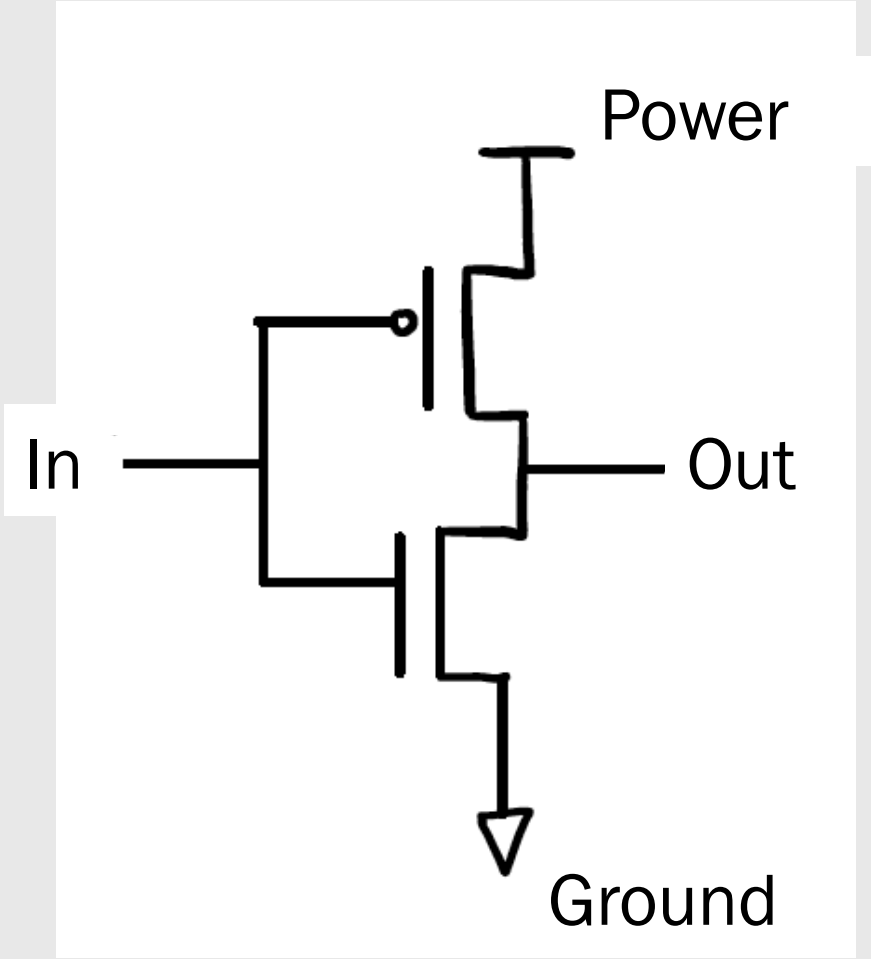


Should this switch be replaced by an nmos or pmos transistor?

Should this switch be replaced by an nmos or pmos transistor?

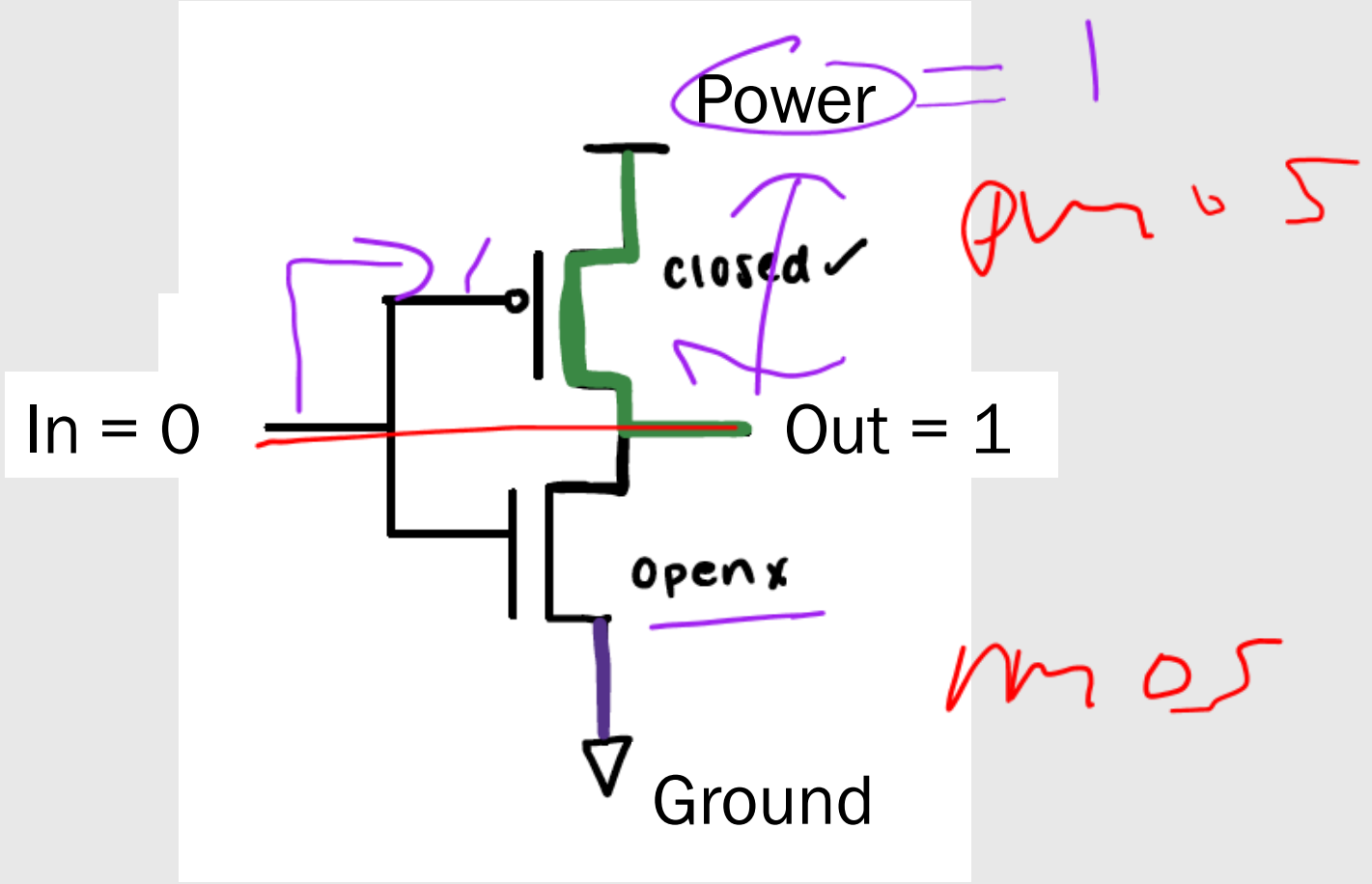
CMOS Inverter

In	Out
0	1
1	0



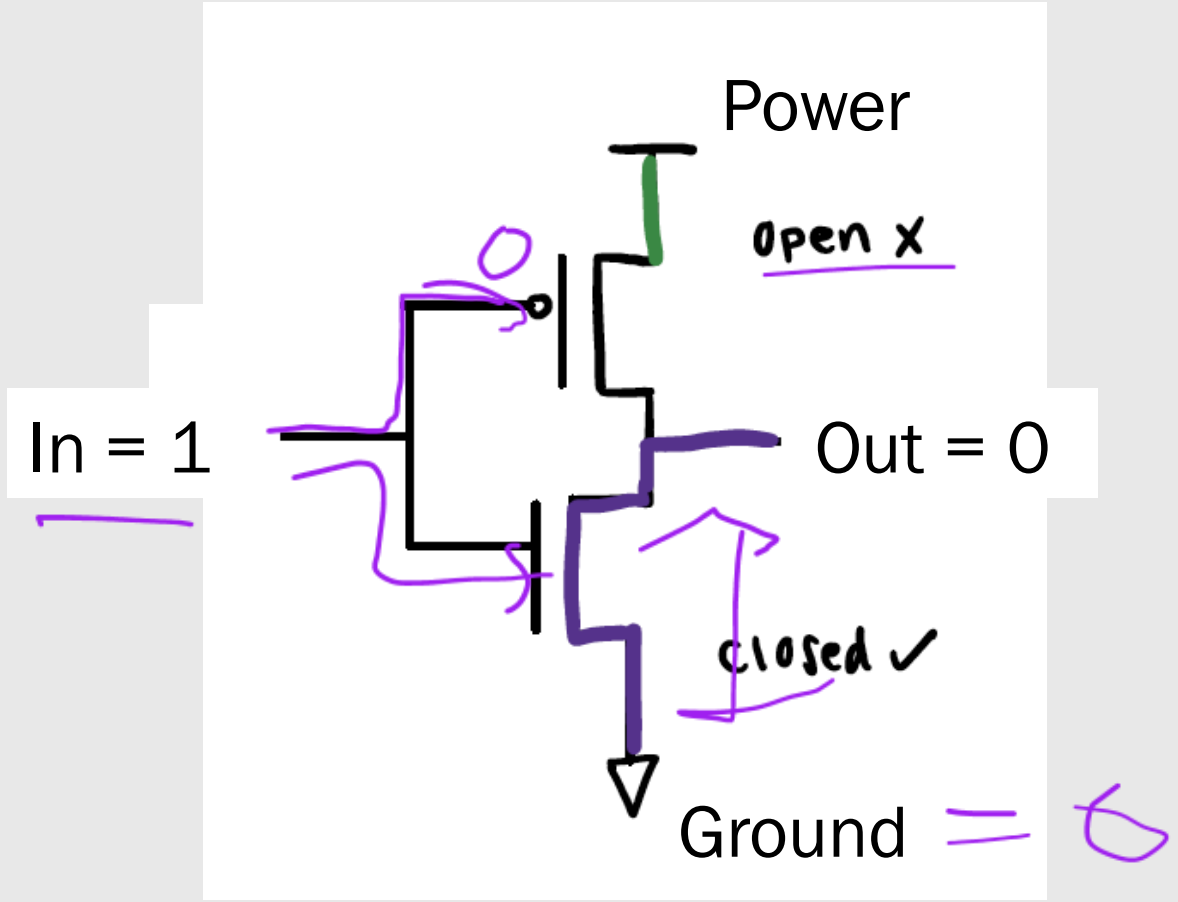
CMOS Inverter

In	Out
0	1
1	0



CMOS Inverter

In	Out
0	1
1	0



CMOS Gates

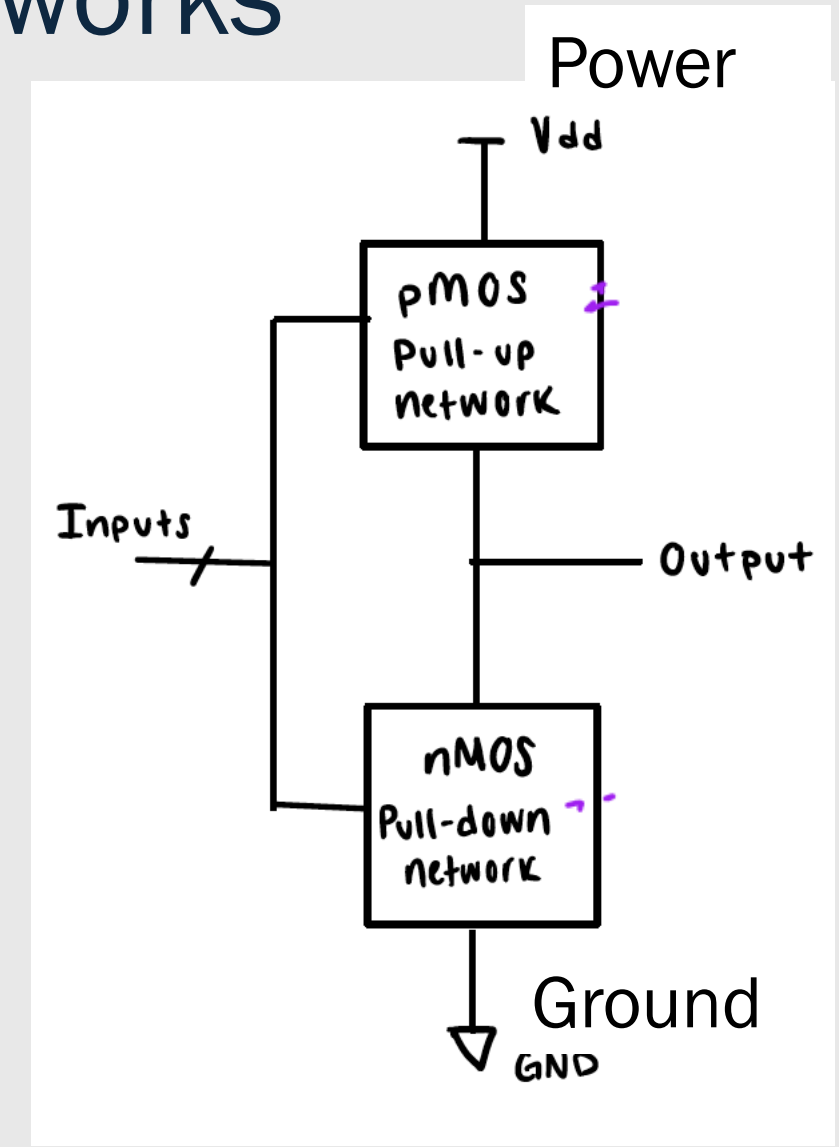
- CMOS = Complementary MOS
  - *The pMOS and nMOS transistors complement each other to form the logic gate*
- Common confusion
  - *CMOS is not a type of transistor!*
  - *It is a technology that combines both nMOS and pMOS transistors*

***MOS*: Metal Oxide Semiconductor ☺**

You might also see ***MOSFET:*** Metal Oxide Semiconductor Field-Effect Transistor

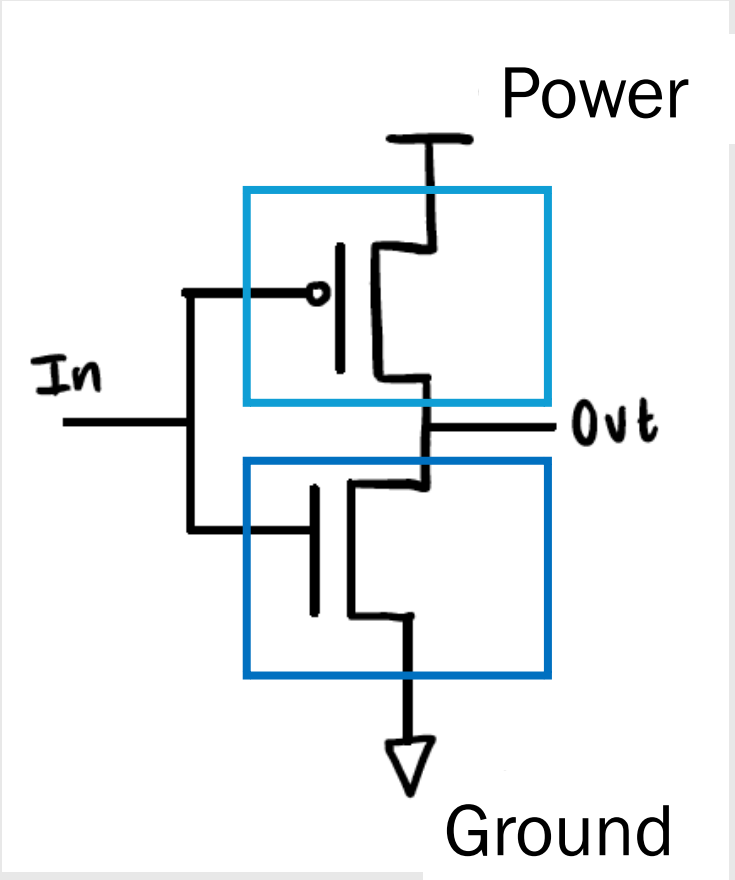
Pull-up and Pull-down Networks

- Only one network will be on at a time
- The pull-up network drives the output when the output is 1
- The pull-down network drives the output when the output is 0



CMOS Inverter

In	Out
0	1
1	0



pull-up network

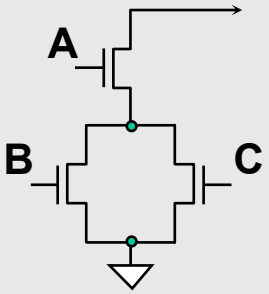
pull-down network

General CMOS Gate Recipe

nMOS

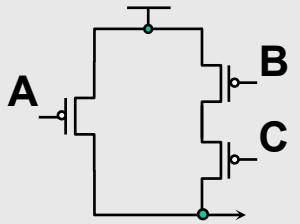
Step 1. Figure out pulldown network that does what you want (i.e the set of conditions where the output is '0')

e.g., F = A*(B+C)



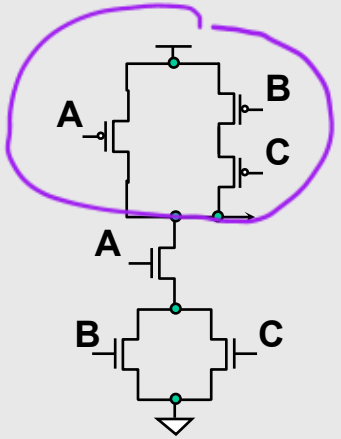
Recall:
Series = *AND*
Parallel = *OR*

Step 2. Build the "opposite" version of that network to figure out when the output should be 1.



This comes from DeMorgan's Laws! In practice, we swap series + parallel connections, use pMOS instead of nMOS

Step 3. Combine the two so you have a circuit that always pulls the output either up to 1 or down to 0.

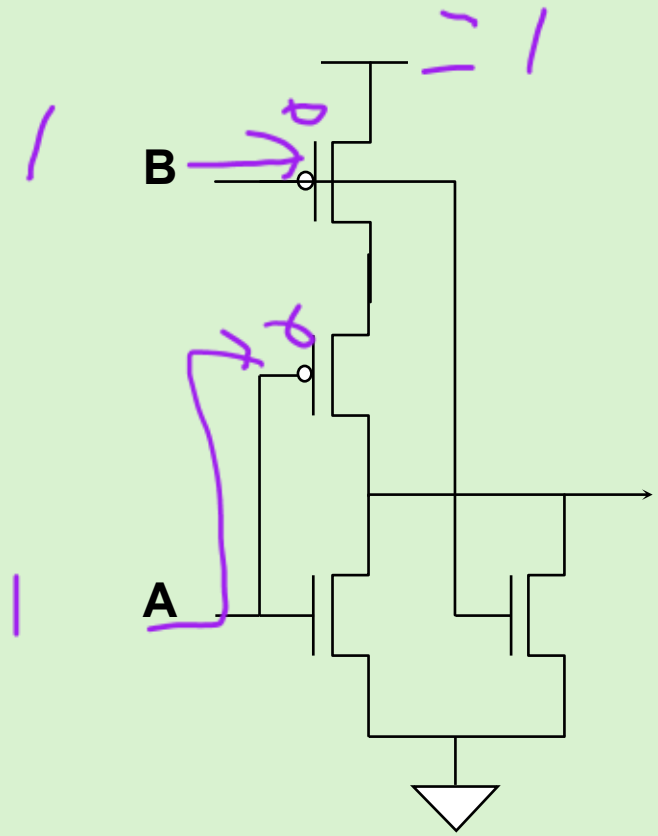


But isn't it hard to wire it all up?

Yes it is! This does not scale...

32

What function does this gate compute?



A	B	C
0	0	1
0	1	0
1	0	0
1	1	0