COMP311: *COMPUTER ORGANIZATION!*

Lecture 7: Gate Minimization Pt. 2

tinyurl.com/comp311-sp26

Logistics Updates

- First lab out
- WA2 out!
- Support email!
  - *comp311-sp26-cs@cs.unc.edu*

GATE MINIMIZATION

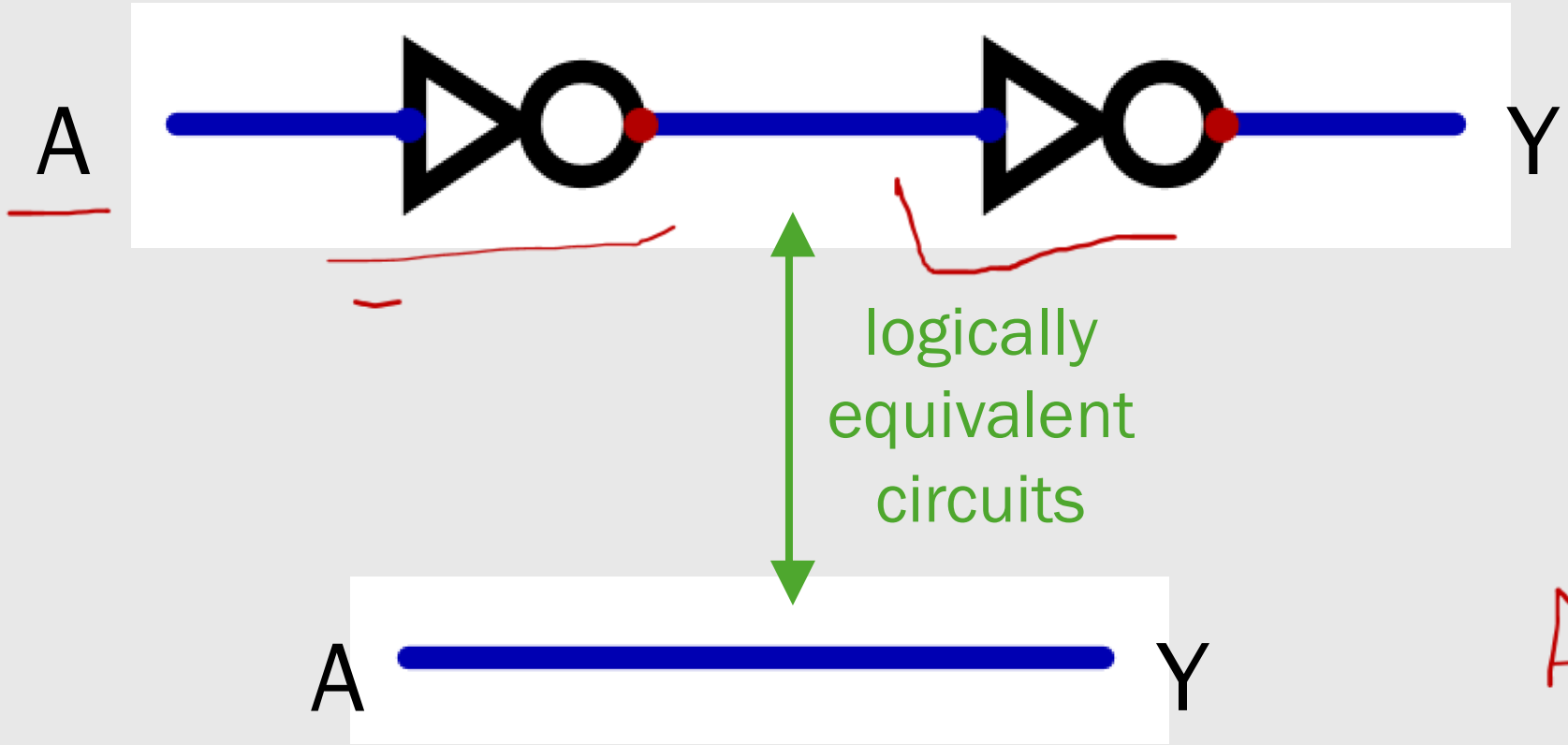
Optimizing our circuits…

- Fewer transistors means….
  - *Smaller area!*
  - *Lower power consumption!*
  - *Shorter time from input to output!*
  - *Lower cost!*
- How will we do this?
  - *Visual inspection*
  - *Boolean algebra simplification*
  - *In practice, → advanced synthesis algorithms to create **logically equivalent,** more efficient circuits!* ☺

Strategies for Minimizing Circuits

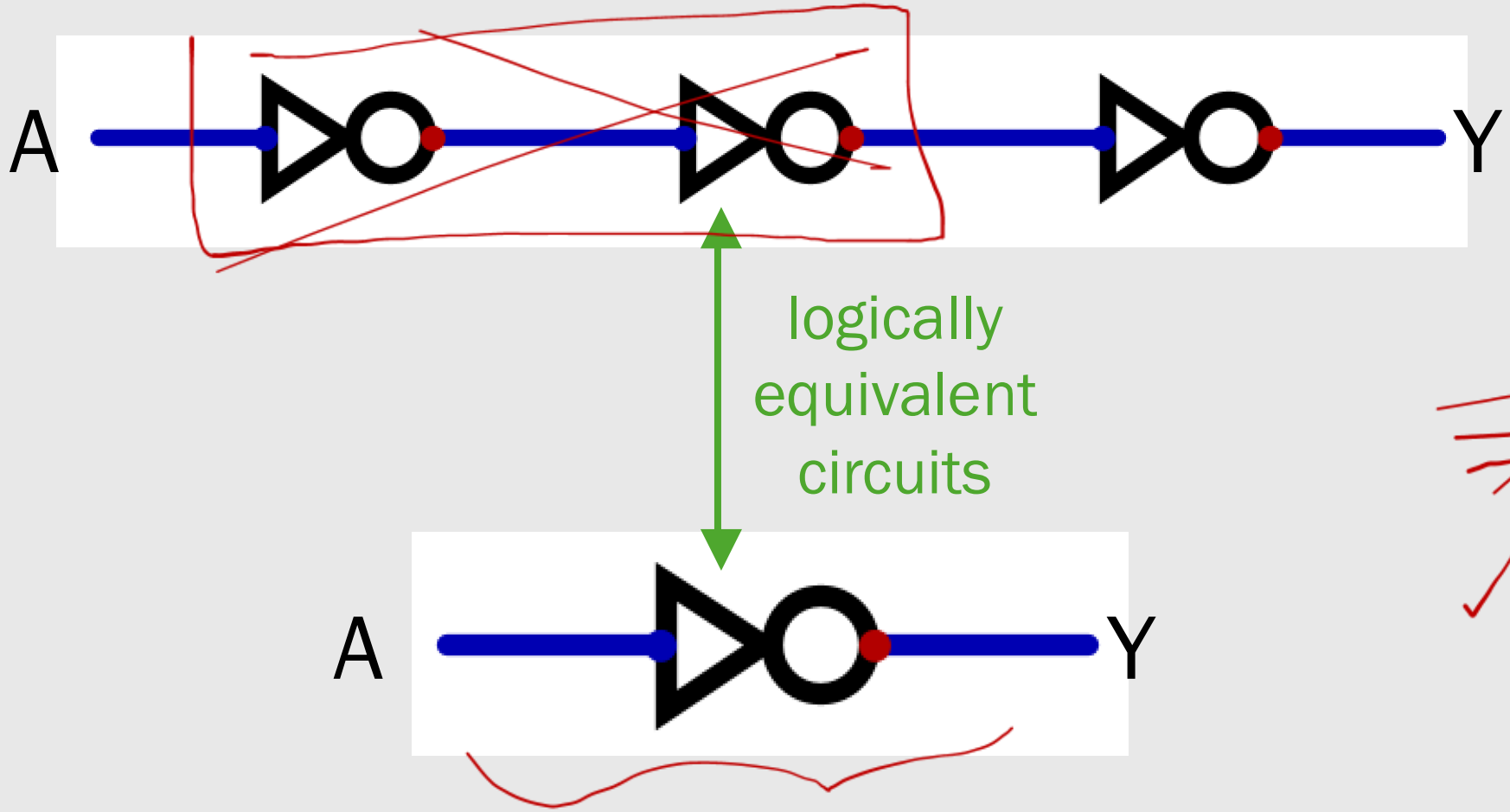
- Deriving a **logically equivalent circuit** that uses **fewer transistors**
- What does logically equivalent mean?
  - *For any input, they will produce the same output*
  - *In other words, their truth tables are equivalent!*

Inverters



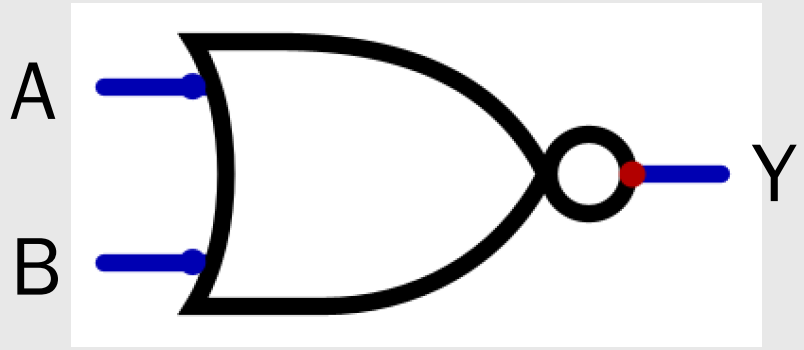
Any even number of inverters chained together is logically equivalent to having no inverters

Inverters

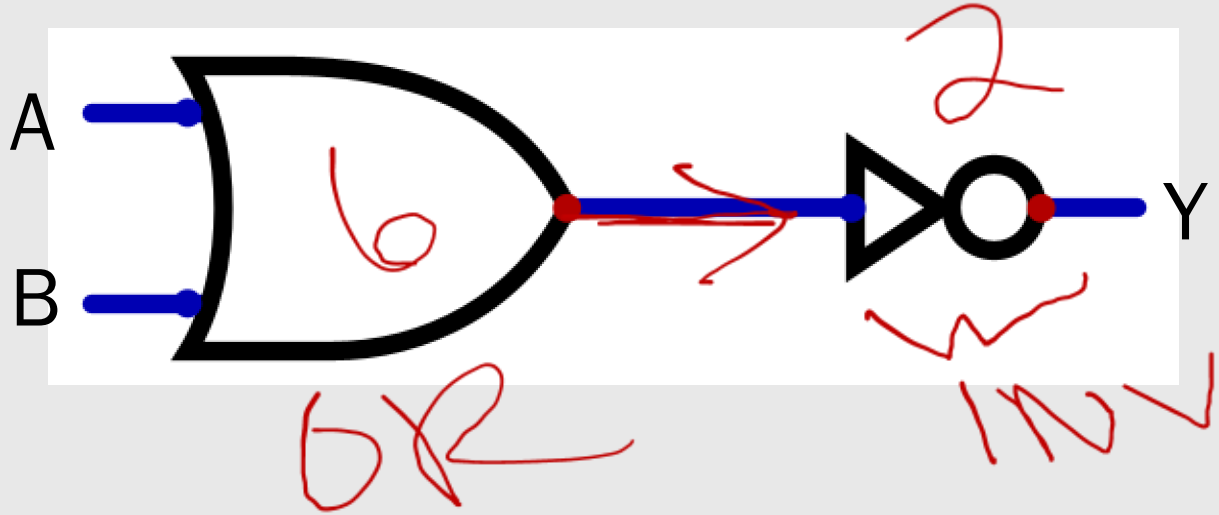


Any odd number of inverters chained together is logically equivalent to having one inverter

A Bubble is Logically Equivalent to Inverter

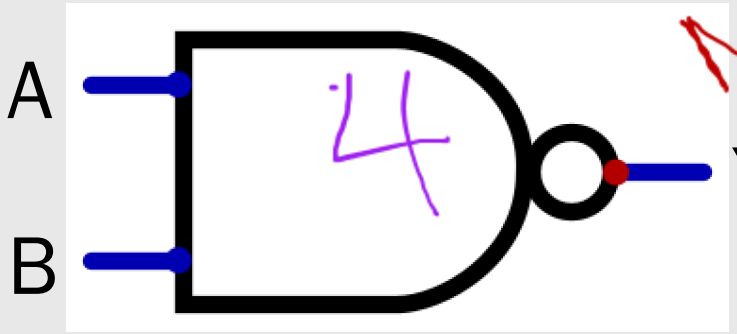


4 transistors

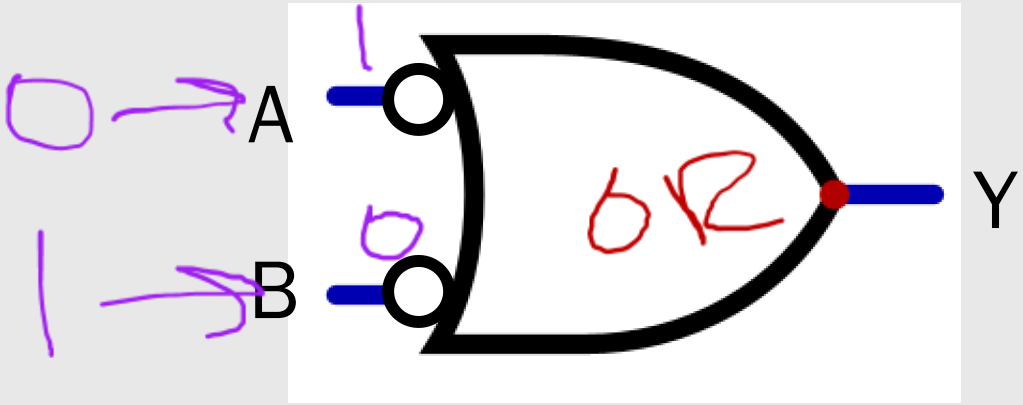


8 transistors

NAND == Inverted OR

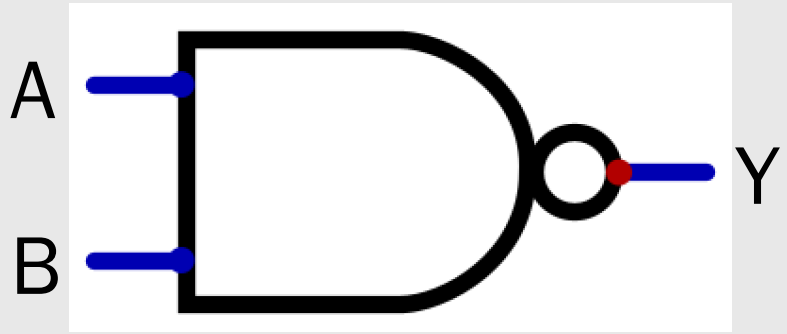


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

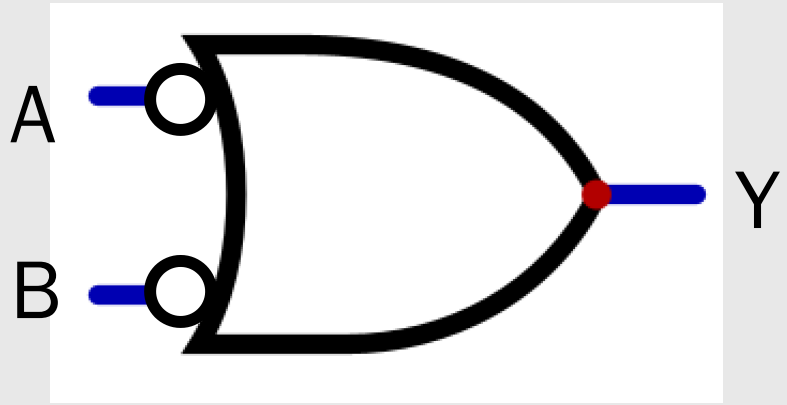


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NAND == Inverted OR

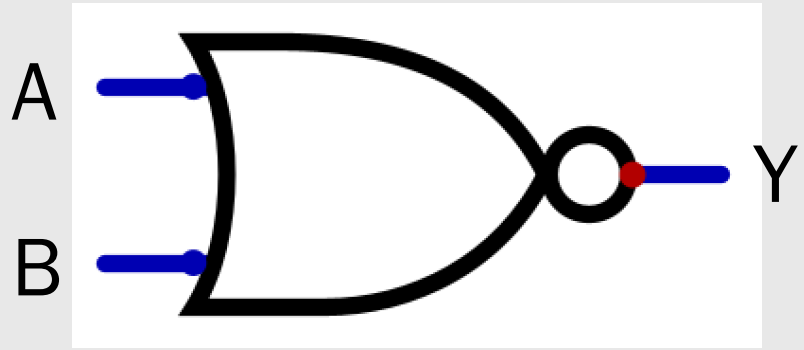


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

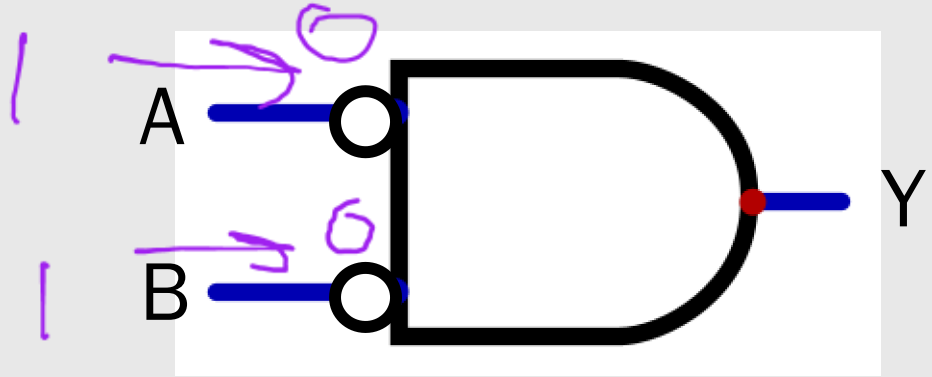


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR == Inverted AND

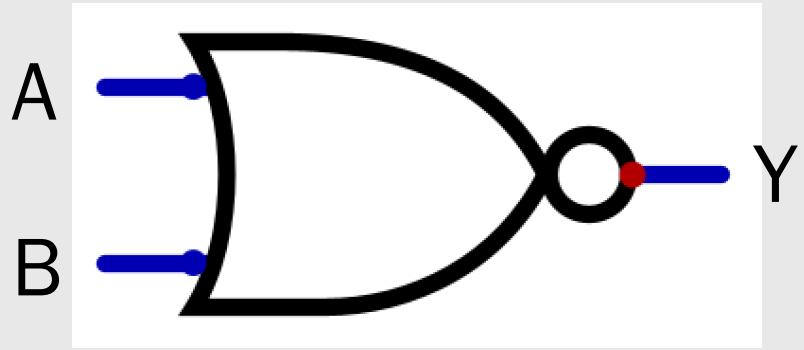


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

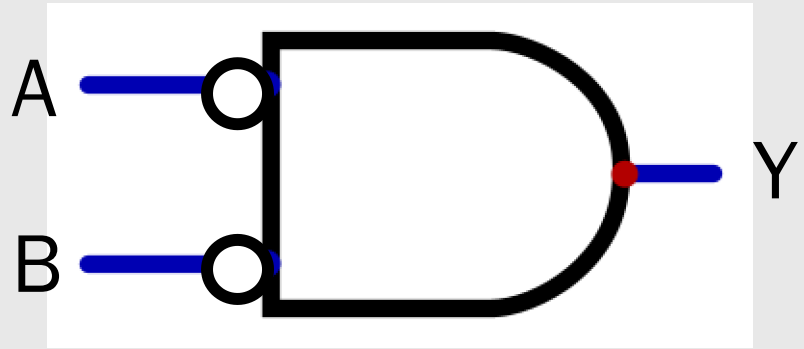


A	B	Y
0	0	
0	1	
1	0	
1	1	0

NOR == Inverted AND



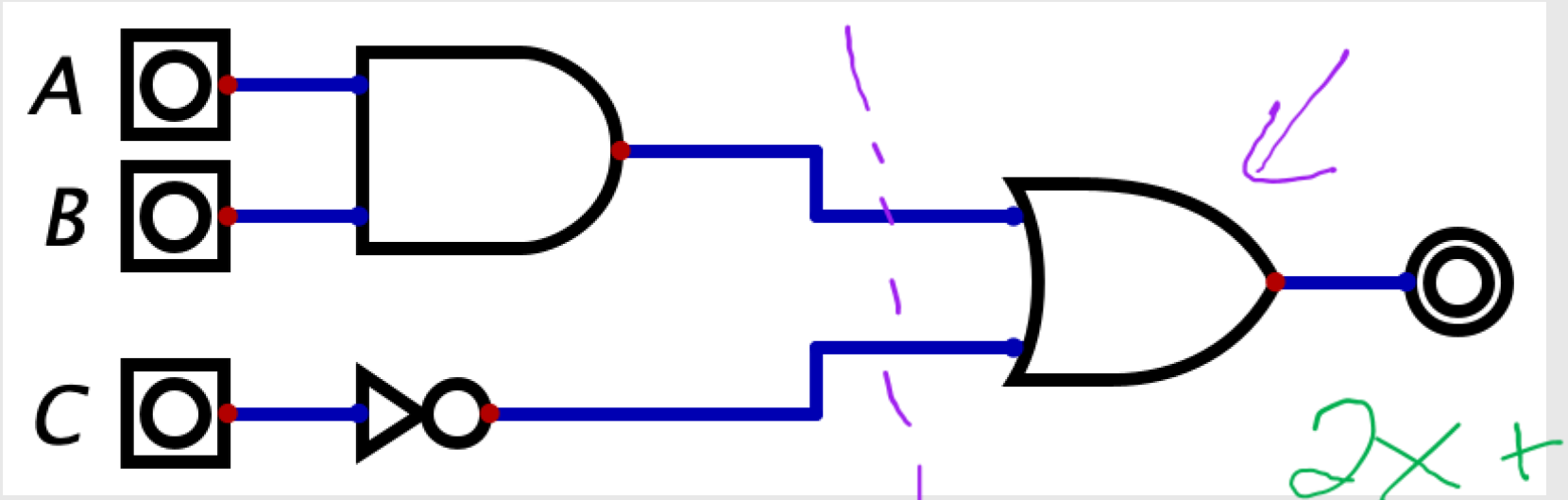
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



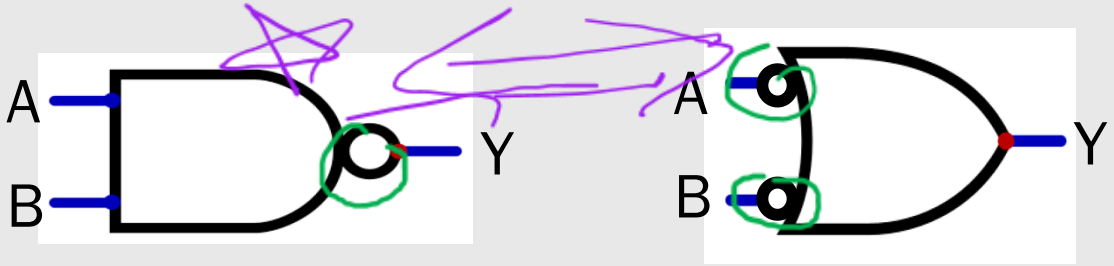
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Ex1: Minimizing Transistor Count

Minimize the number of transistors in this circuit by redesigning it to use only NAND gates and inverters.

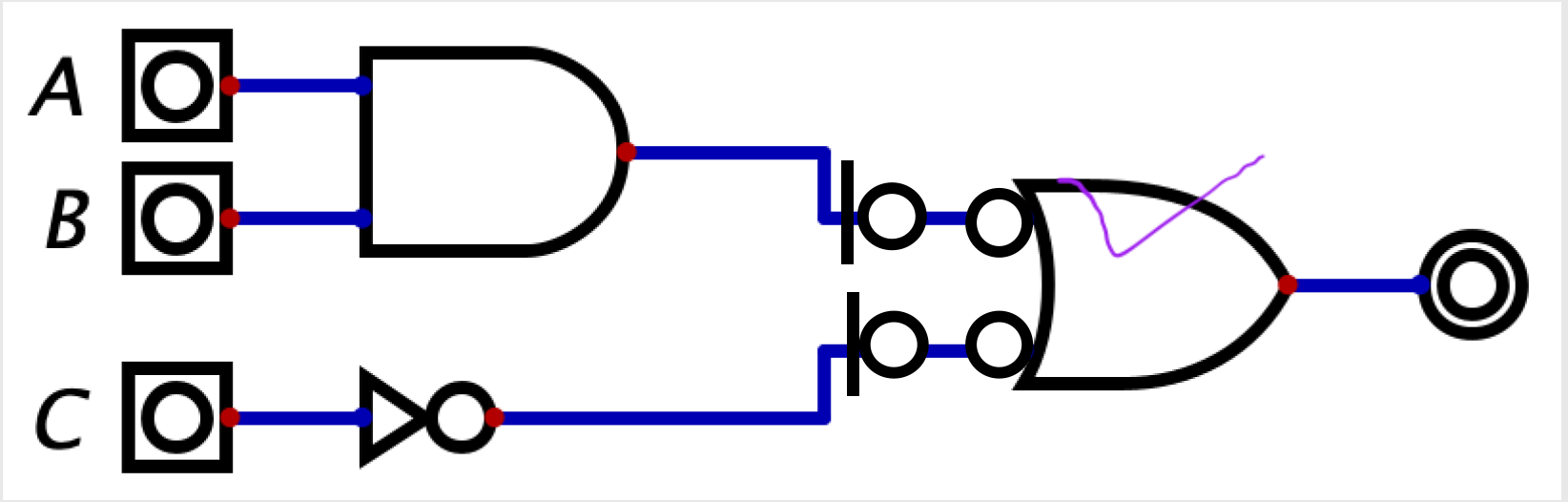


NAND gates:

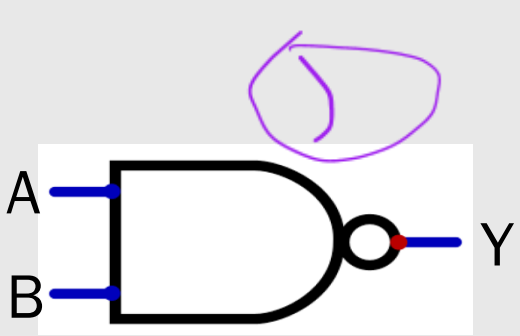


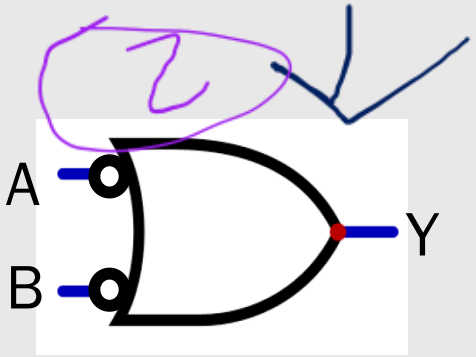
Ex1: Minimizing Transistor Count

Step 1: Start with the right-most gate. Turn it into a NAND gate. Then add bubbles to make the circuit logically equivalent.



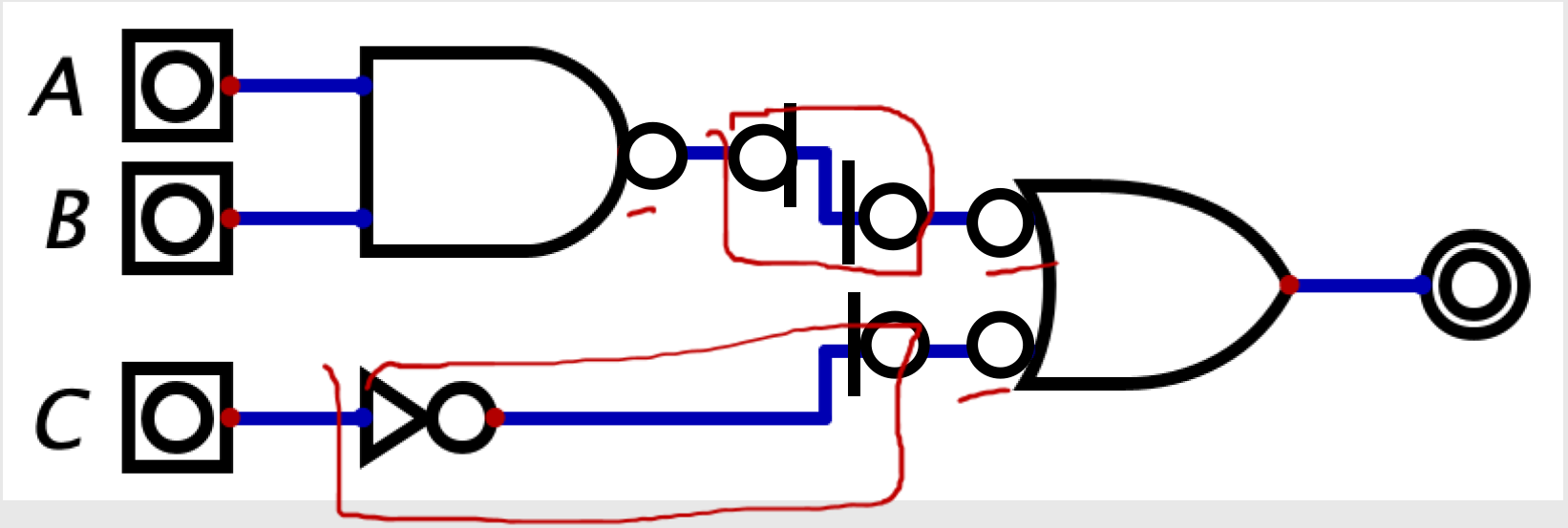
NAND gates:



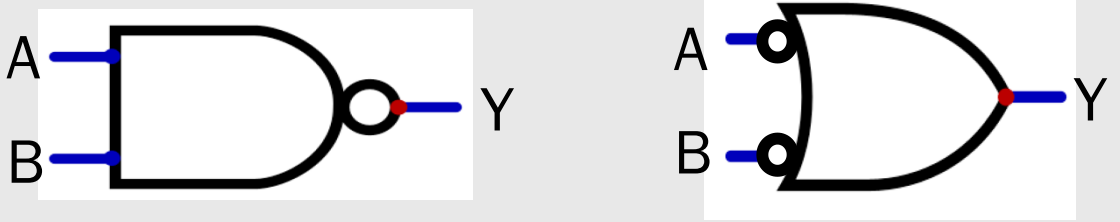


Ex1: Minimizing Transistor Count

Step 2: Now make the top left gate a NAND gate. Then add a bubble to make the circuit logically equivalent.

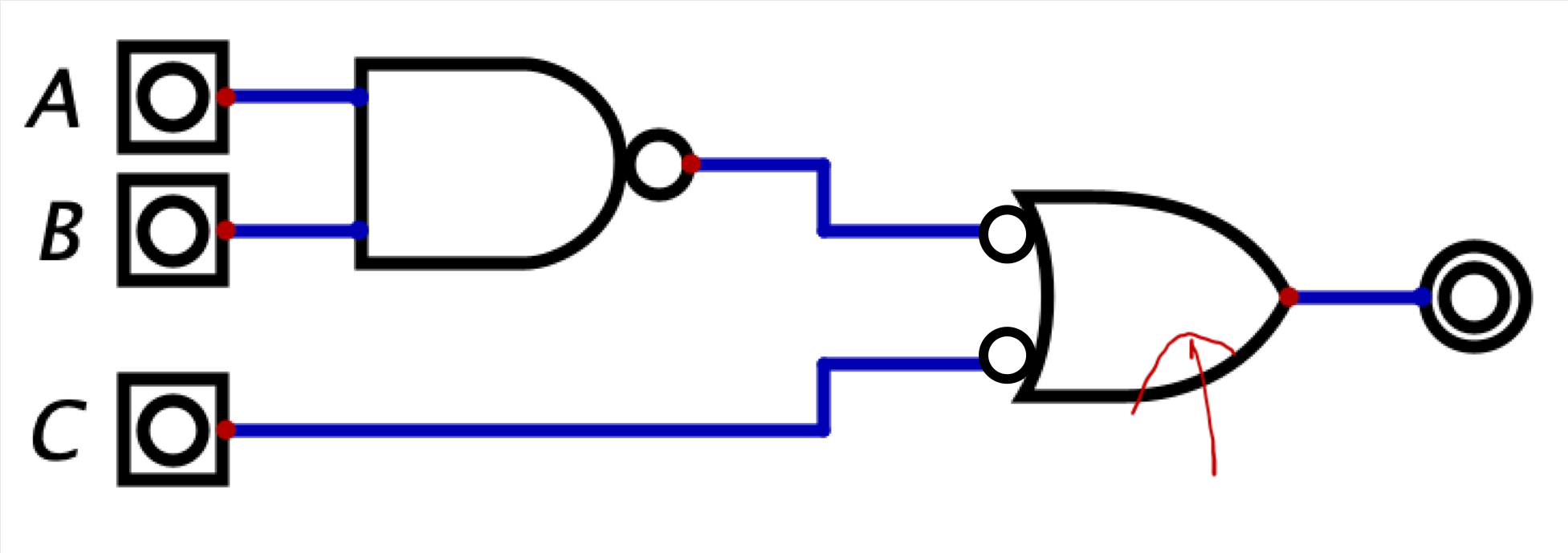


NAND gates:



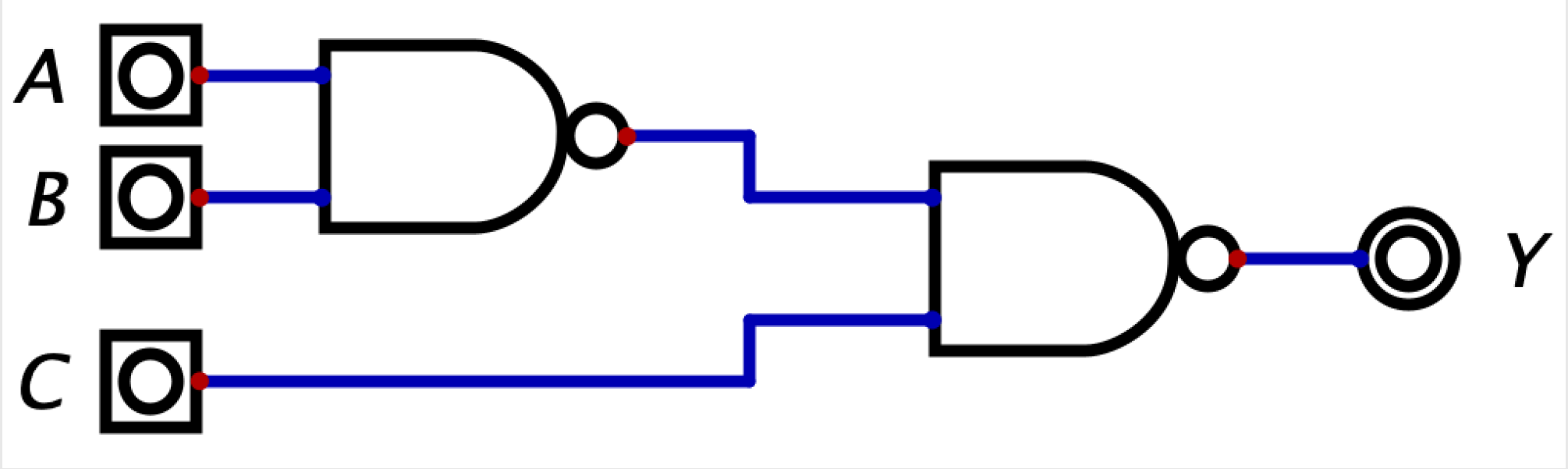
Ex1: Minimizing Transistor Count

Step 3: Cancel out the free bubbles. (Pairs of inverters/bubbles cancel!)



Ex1: Minimizing Transistor Count

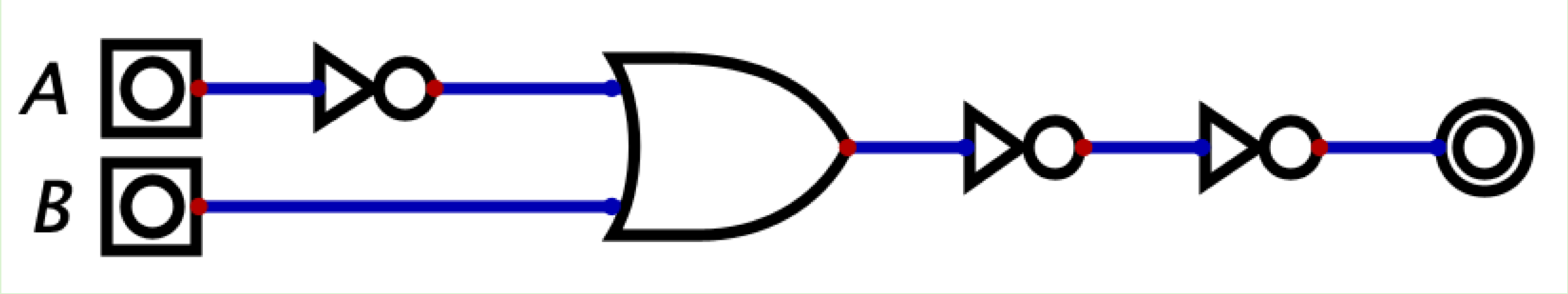
Step 4: Draw the gates in their conventional form.



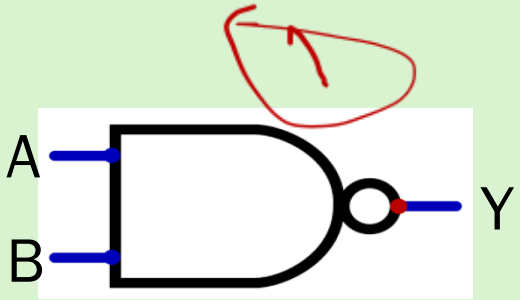
Original Transistor Count: 14
Final Transistor Count: 8

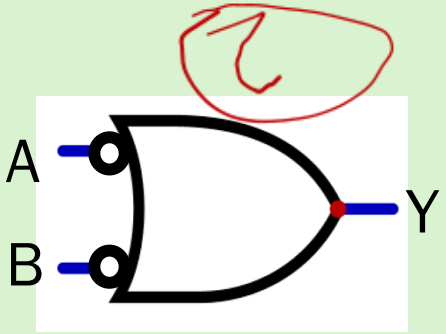
Minimizing Transistor Count

Minimize the number of transistors in this circuit by redesigning it to use only NAND gates and inverters. Compare the number of transistors in the original circuit and the new circuit.



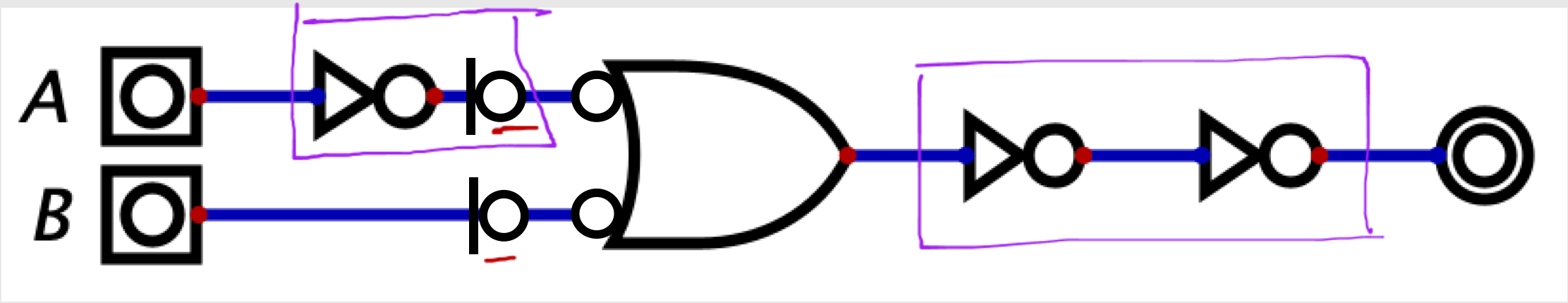
NAND gates:



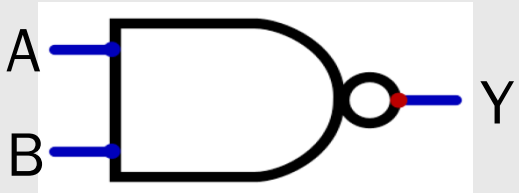


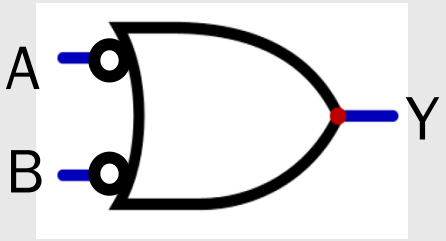
Minimizing Transistor Count

Step 1: Transform the OR gate into a NAND gate. Add bubbles to make the circuit logically equivalent.



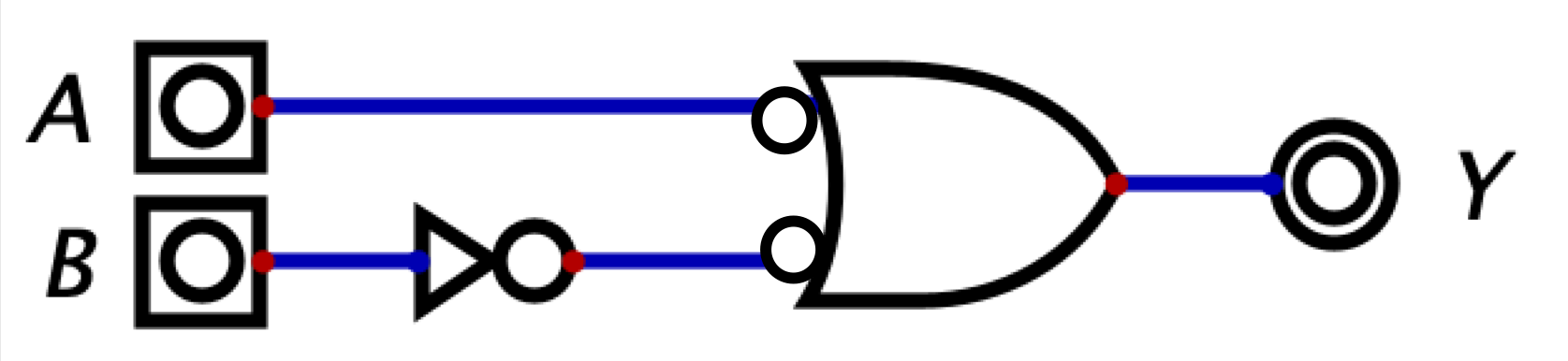
NAND gates:





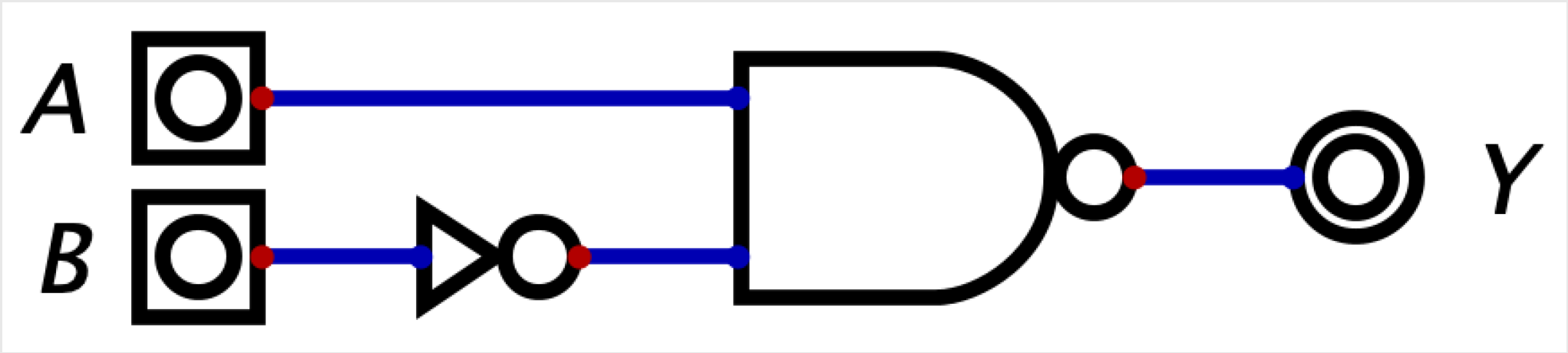
Minimizing Transistor Count

Step 2: Cancel out extra bubbles and inverters.



Minimizing Transistor Count

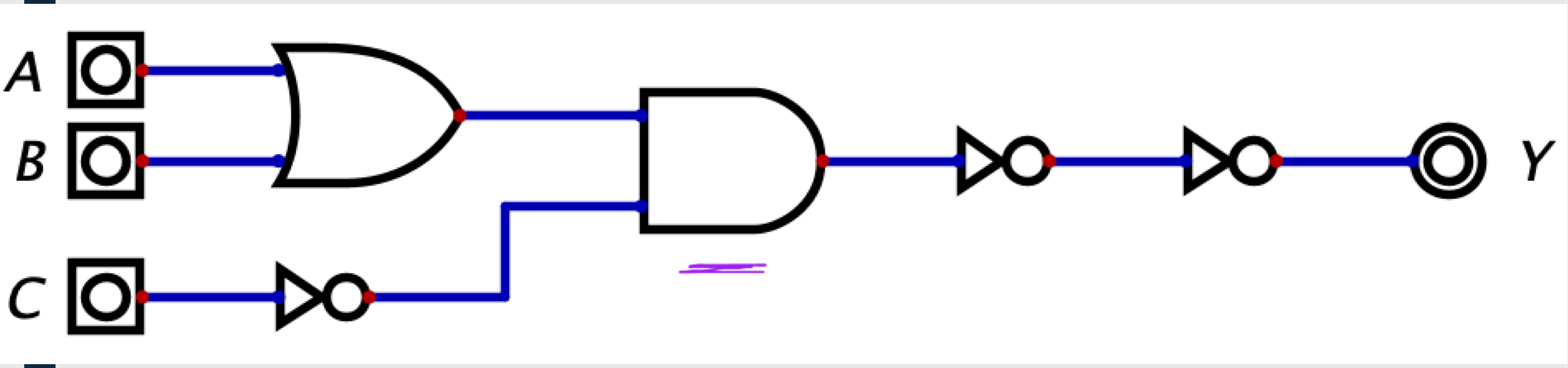
Step 3: Draw the gates in their conventional form.



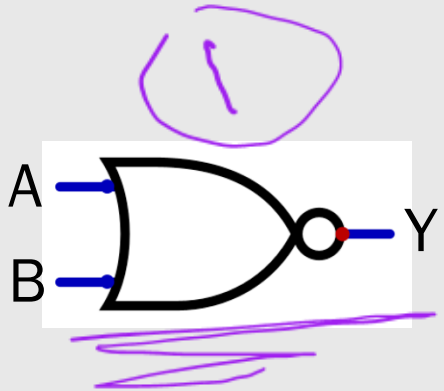
Original Transistor Count: 12
Final Transistor Count: 6

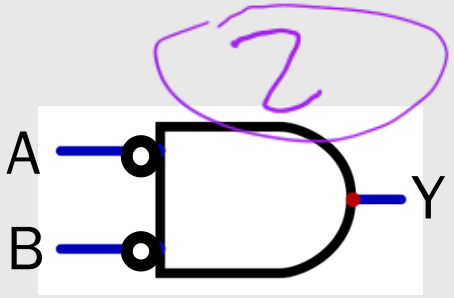
Ex2: Minimizing Transistor Count

Minimize the number of transistors in this circuit by redesigning it to use only NOR gates and inverters.



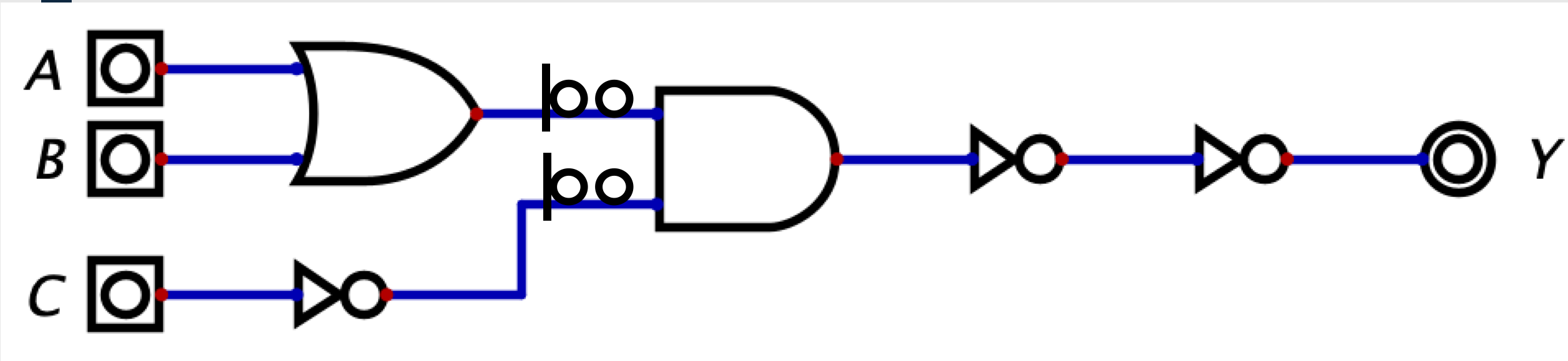
NOR gates:



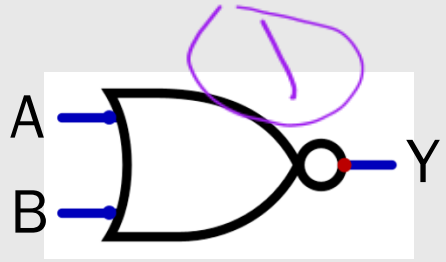


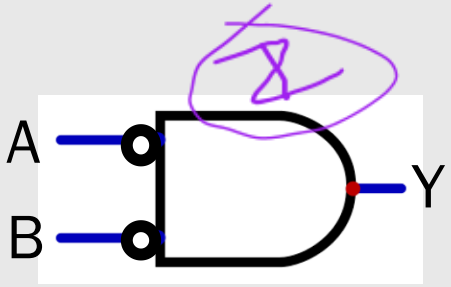
Ex2: Minimizing Transistor Count

Step 1: Start with the right-most gate that is not an inverter. Turn it into a NOR gate. Then add bubbles to make the circuit logically equivalent.



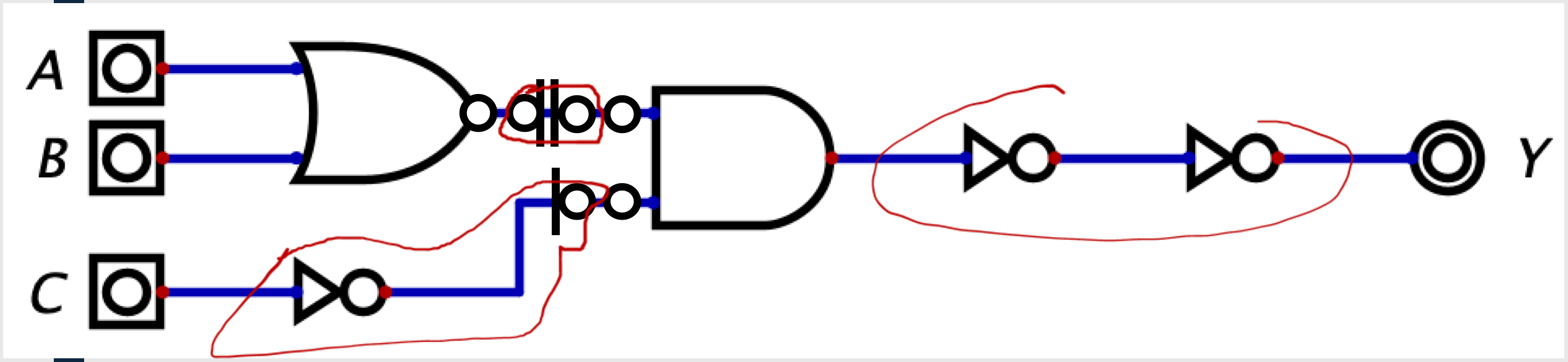
NOR gates:



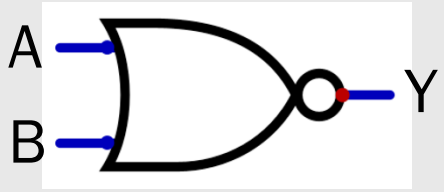


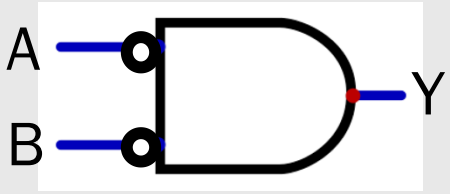
Ex2: Minimizing Transistor Count

Step 2: Move to the next gate on the left. Transform this into a NOR gate. Add a bubble to make the circuit logically equivalent.



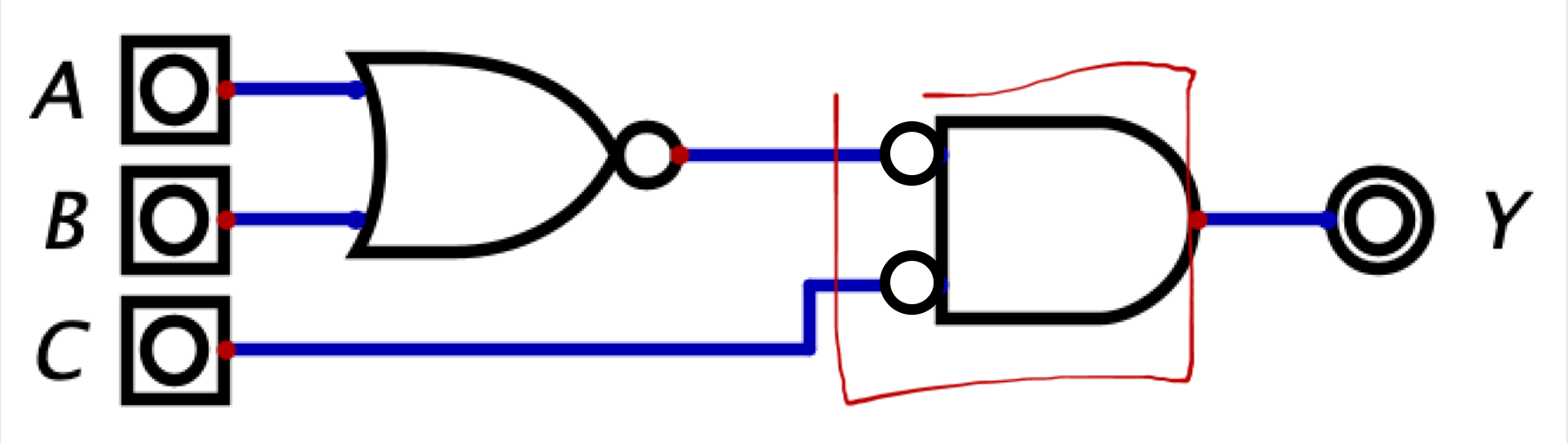
NOR gates:





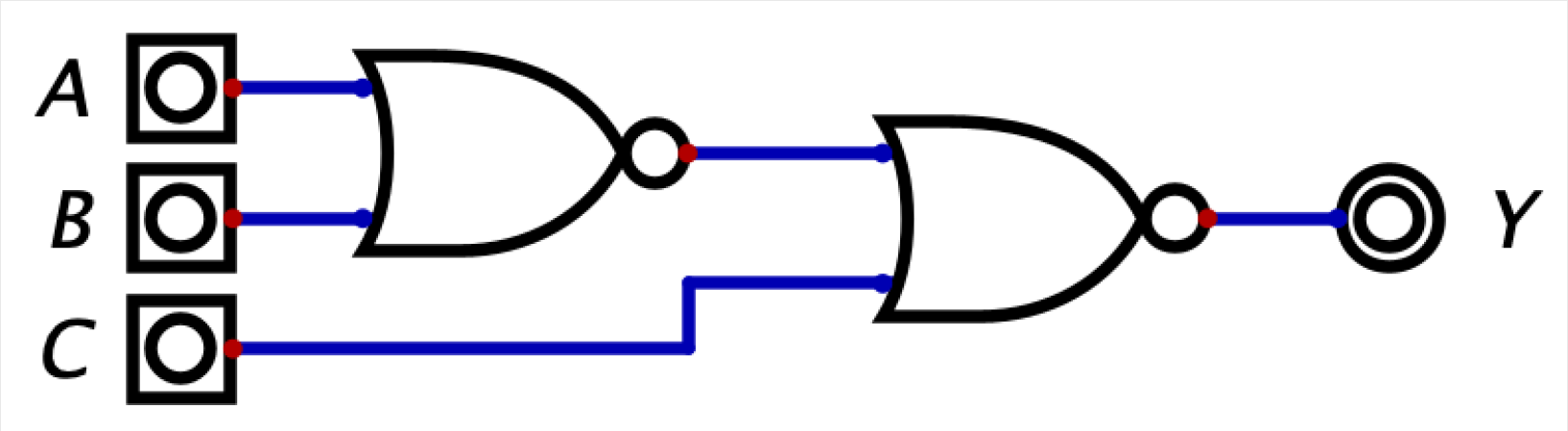
Ex2: Minimizing Transistor Count

Step 3: Cancel out the extra bubbles and inverters.



Ex2: Minimizing Transistor Count

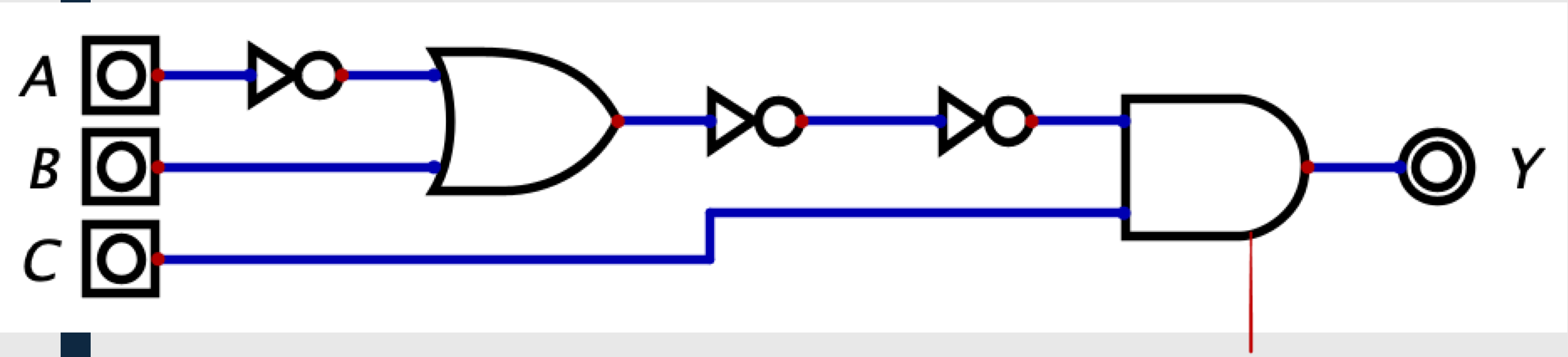
Step 4: Draw the gates in their conventional form.



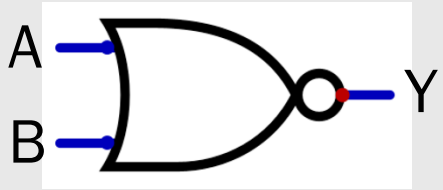
Original Transistor Count: 18
Final Transistor Count: 8

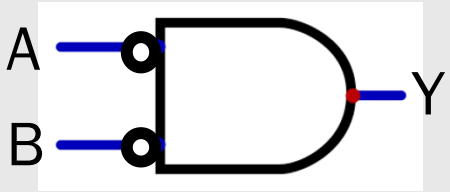
Minimizing Transistor Count

Minimize the number of transistors in this circuit by redesigning it to use only NOR gates and inverters. Compare the number of transistors in the original circuit and the new circuit.



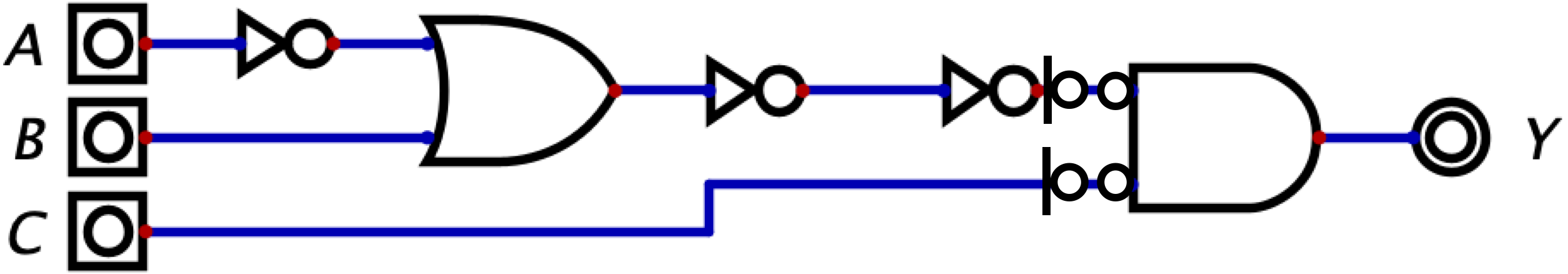
NOR gates:



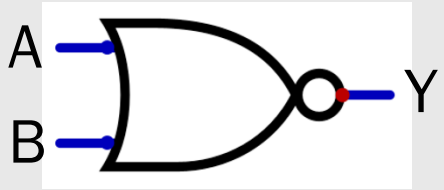


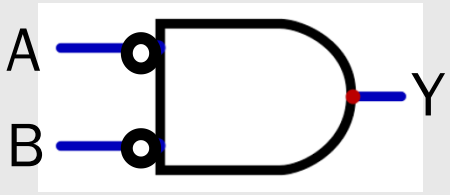
Minimizing Transistor Count

Step 1: Start with the right-most gate. Turn it into a NOR gate. Then add bubbles to make the circuit logically equivalent.



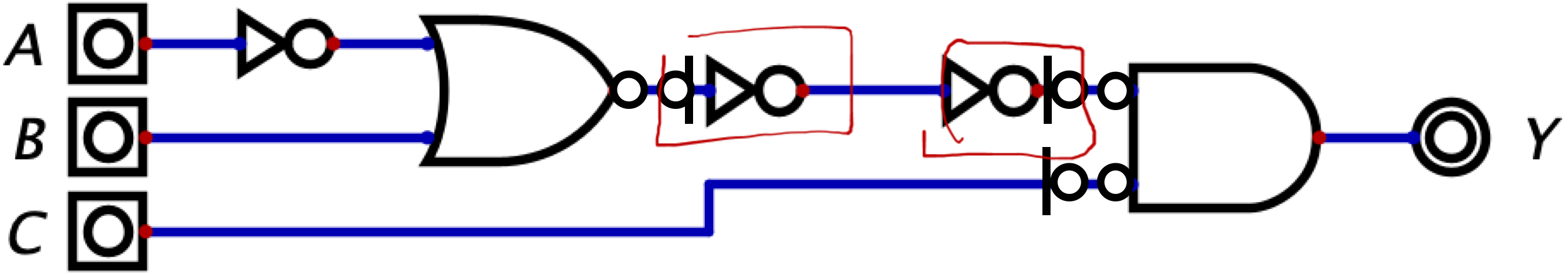
NOR gates:



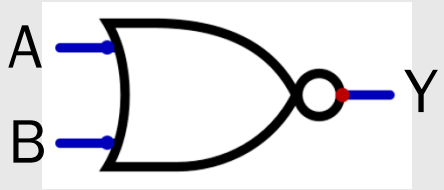


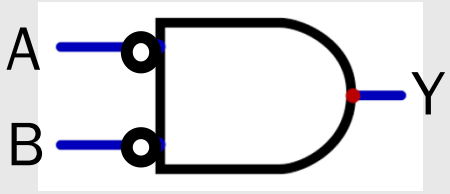
Minimizing Transistor Count

Step 2: Move to the next gate on the left. Transform this into a NOR gate. Add a bubble to make the circuit logically equivalent.



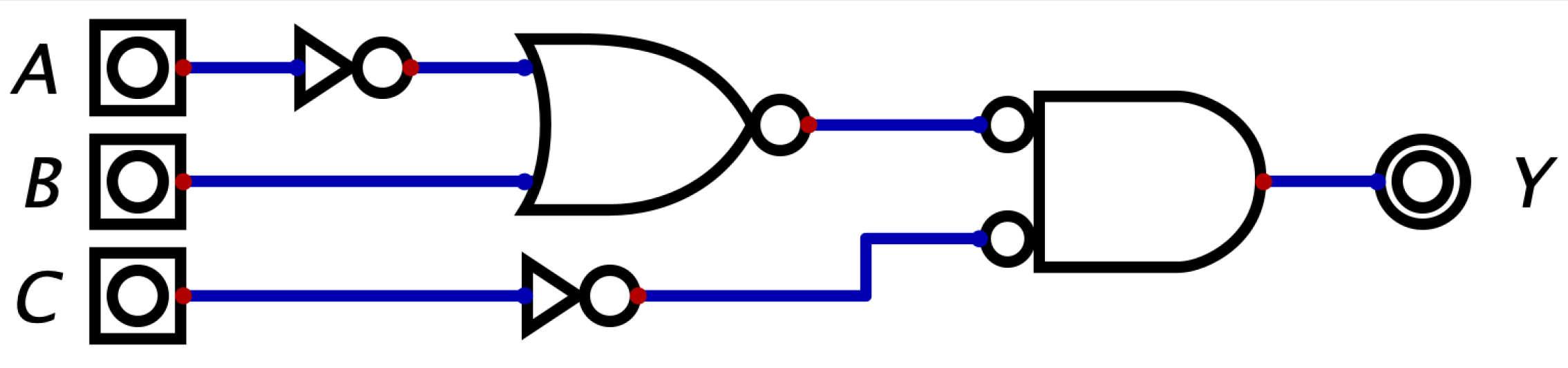
NOR gates:





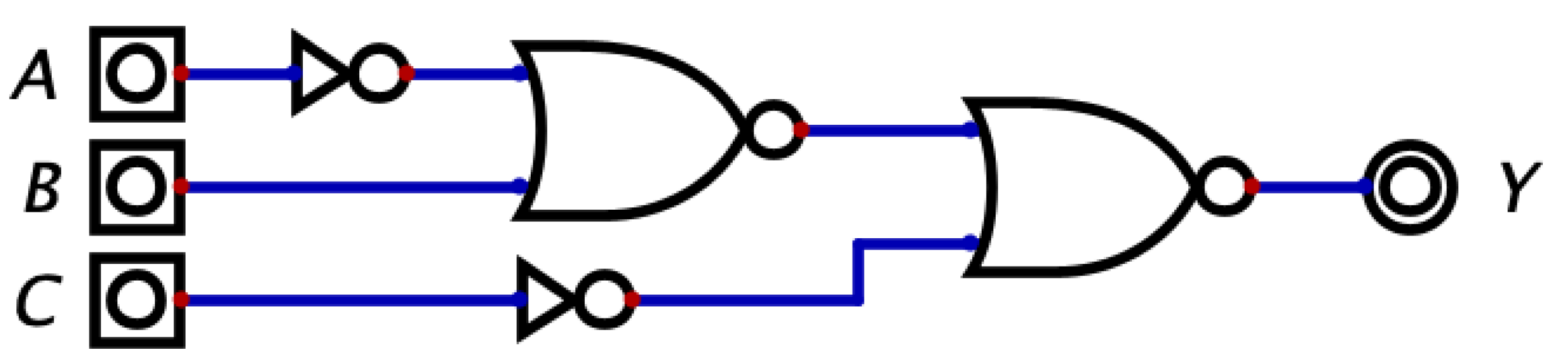
Minimizing Transistor Count

Step 3: Cancel out the extra bubbles and inverters.



Minimizing Transistor Count

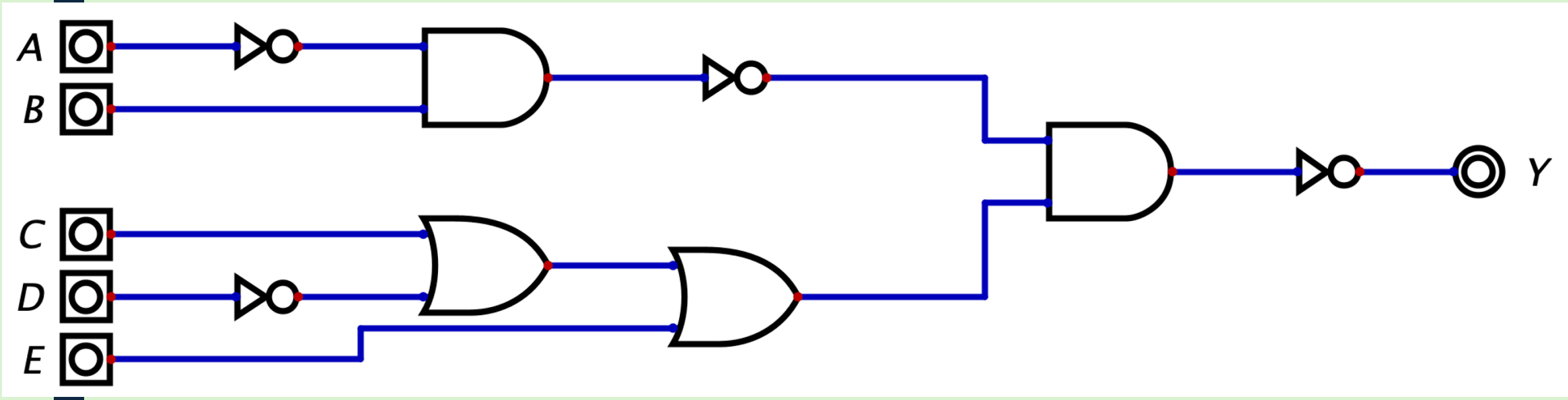
Step 4: Draw the gates in their conventional form.



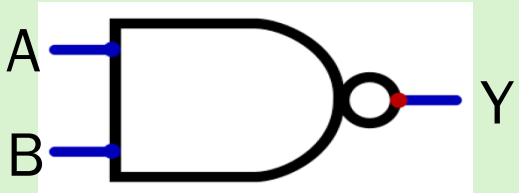
Original Transistor Count: 18
Final Transistor Count: 12

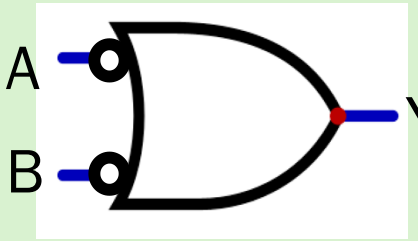
Minimizing Transistor Count

Minimize the number of transistors in this circuit by redesigning it to use only NAND gates and inverters. Compare the number of transistors in the original circuit and the new circuit.



NAND gates:





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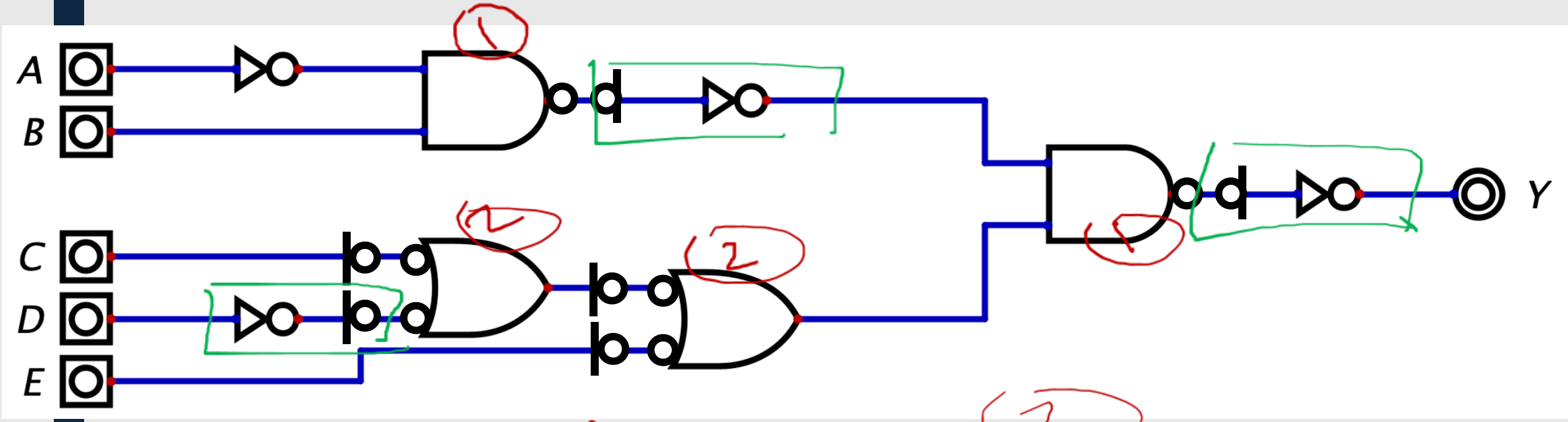
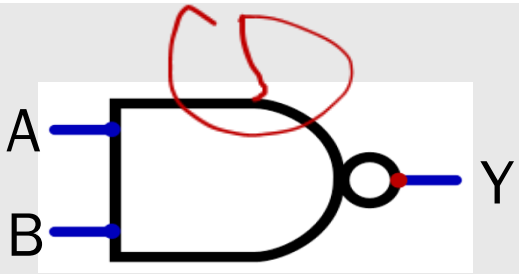
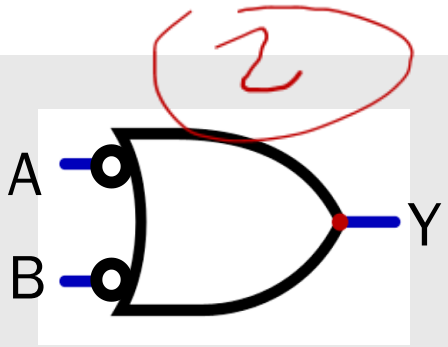


NAND gates:





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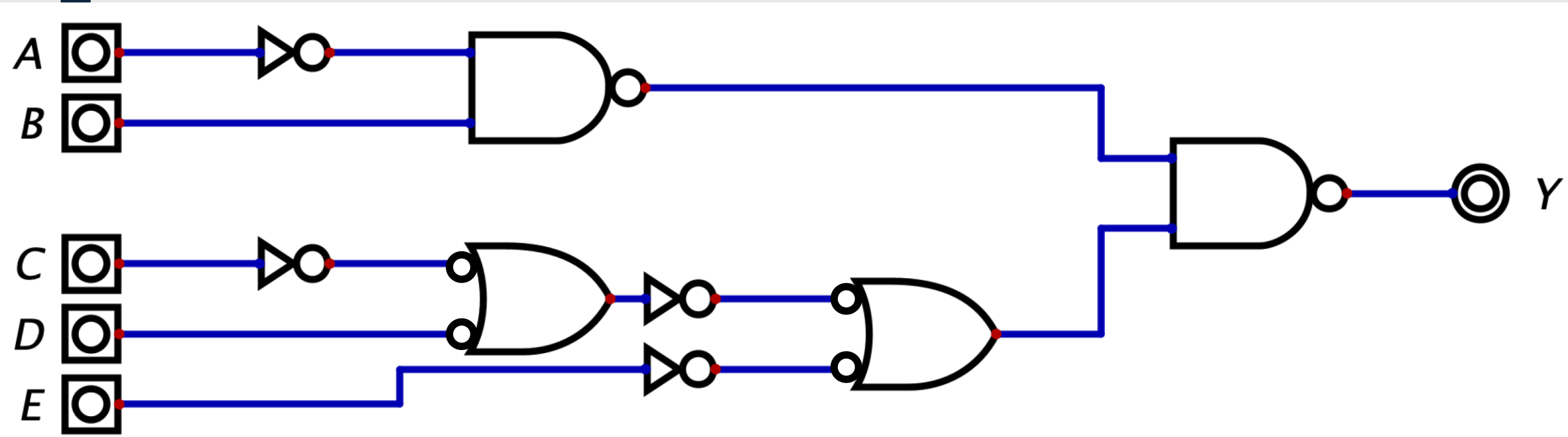
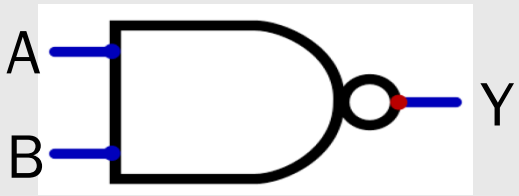
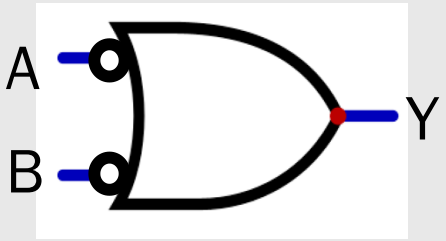


NAND gates:





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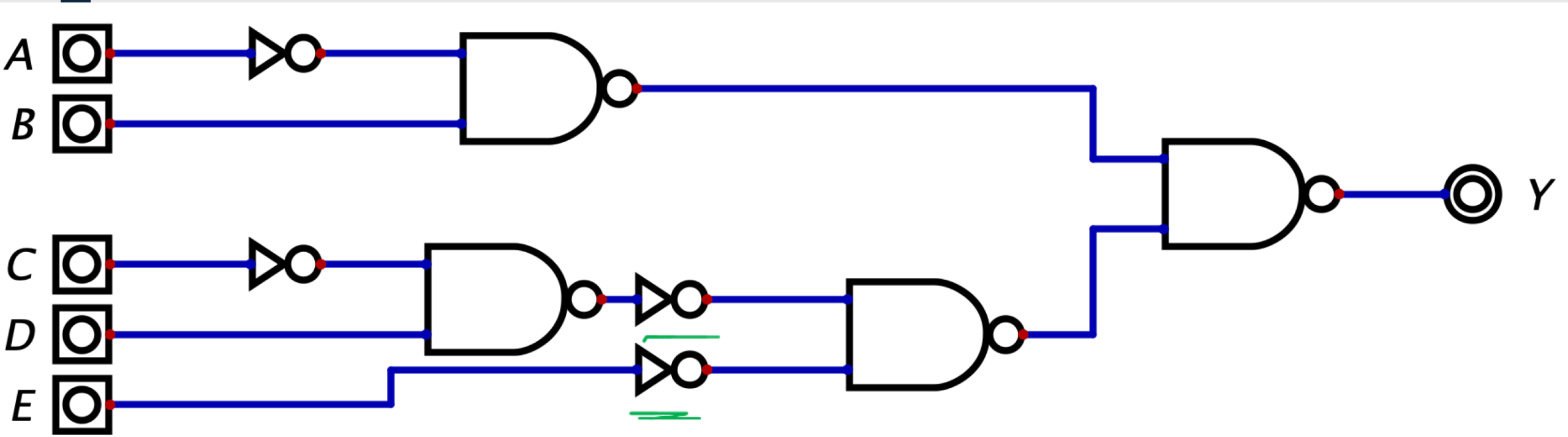
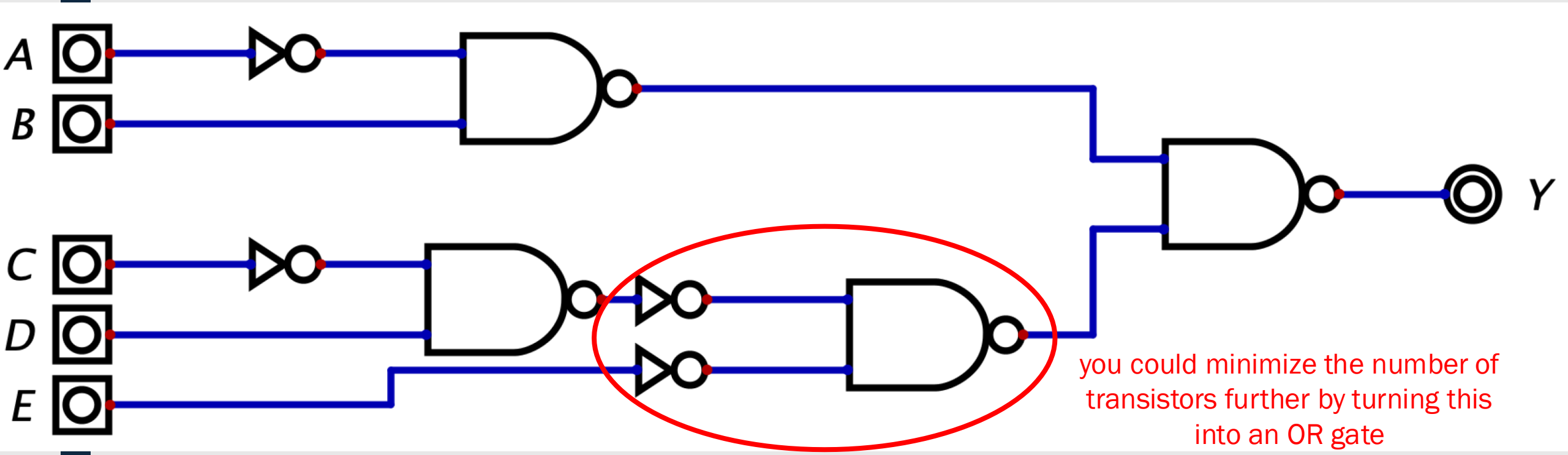


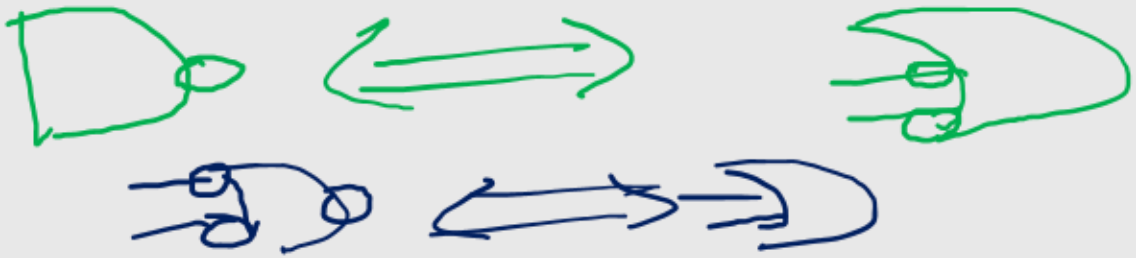
Original Transistor Count: 32

Final Transistor Count: 24

Minimizing Transistor Count

Minimize the number of transistors in this circuit by redesigning it to use only NAND gates and inverters. Compare the number of transistors in the original circuit and the new circuit.





Minimizing Transistor Count

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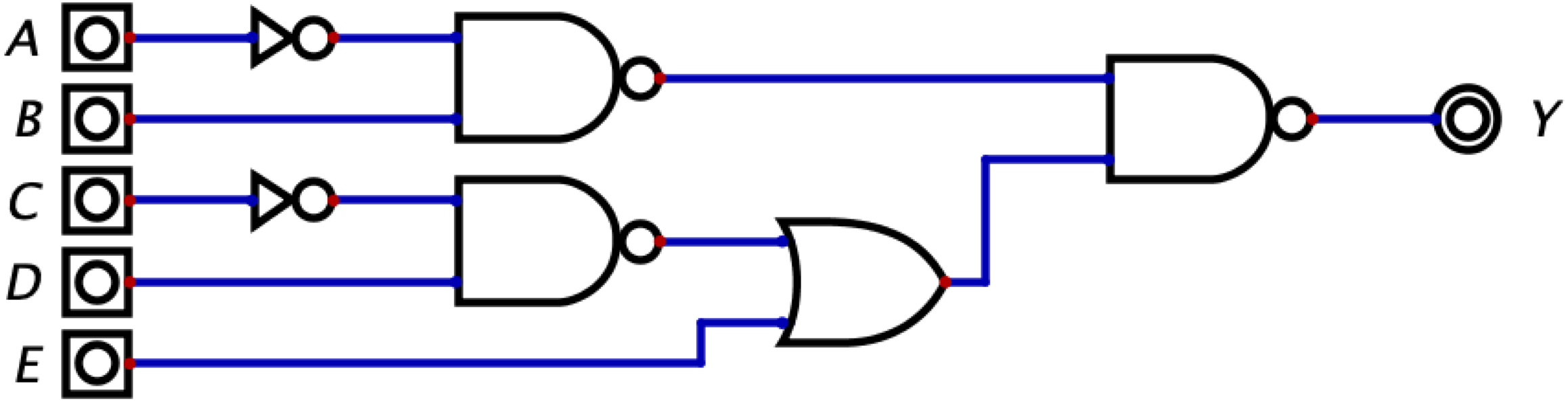

Original Transistor Count: 32

Final Transistor Count: 22