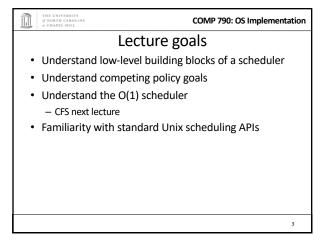


COMP 790: OS Implementation Logical Diagram Memory **Binary** Threads Forp User Today's Lecture Switching to CPU Kernel scheduling orking RCD Sync Memory CPU Device Management Drivers Scheduler Hardware Consistency Interrupts Net

2



**COMP 790: OS Implementation

**COMP 790: OS Implementation

Undergrad review

**What is cooperative multitasking?

- Processes voluntarily yield CPU when they are done

**What is preemptive multitasking?

- OS only lets tasks run for a limited time, then forcibly context switches the CPU

Pros/cons?

- Cooperative gives more control; so much that one task can hog the CPU forever

- Preemptive gives OS more control, more overheads/complexity

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Where can we preempt a process?

In other words, what are the logical points at which the OS can regain control of the CPU?

System calls
Before
During (more next time on this)
After

Interrupts
Timer interrupt – ensures maximum time slice

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(Linux) Terminology

• mm_struct – represents an address space in kernel

• task – represents a thread in the kernel

– A task points to 0 or 1 mm_structs

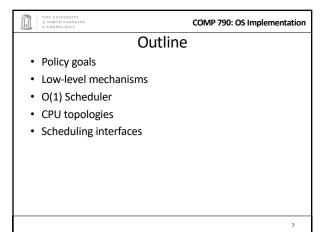
• Kernel threads just "borrow" previous task's mm, as they only execute in kernel address space

– Many tasks can point to the same mm_struct

• Multi-threading

• Quantum – CPU timeslice

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COMP 790: OS Implementation Policy goals • Fairness – everything gets a fair share of the CPU · Real-time deadlines - CPU time before a deadline more valuable than time after • Latency vs. Throughput: Timeslice length matters! - GUI programs should feel responsive - CPU-bound jobs want long timeslices, better throughput User priorities

- Virus scanning is nice, but I don't want it slowing things

Context switching

- Simplified by convention that kernel is at same address

What would be hard about mapping kernel in different

Swap out the address space and running thread



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No perfect solution

- · Optimizing multiple variables
- · Like memory allocation, this is best-effort
 - Some workloads prefer some scheduling strategies

· Nonetheless, some solutions are generally better than others



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Other context switching tasks

- · Swap out other register state
 - Segments, debugging registers, MMX, etc.
- · If descheduling a process for the last time, reclaim its memory
- · Switch thread stacks



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· What is it?

Address space:

places?

 Need to change page tables - Update cr3 register on x86

range in all processes

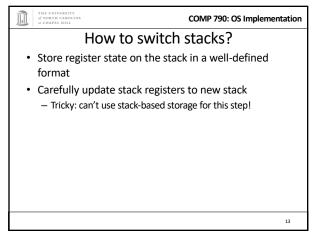
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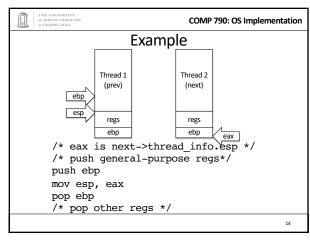
COMP 790: OS Implementation

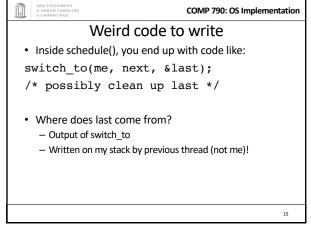
Switching threads

• Programming abstraction:

/* Do some work */ schedule(); /* Something else runs */ /* Do more work */







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How to code this?

Pick a register (say ebx); before context switch, this is a pointer to last's location on the stack

Pick a second register (say eax) to stores the pointer to the currently running task (me)

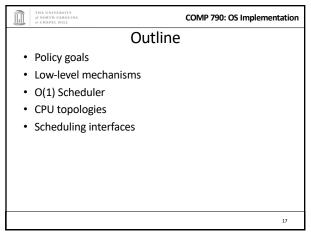
Make sure to push ebx after eax

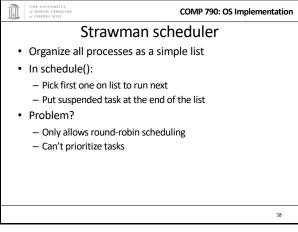
After switching stacks:

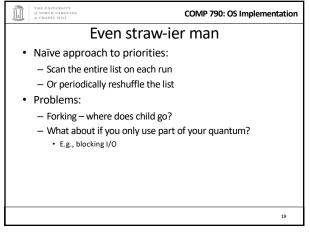
pop ebx /* eax still points to old task*/
mov (ebx), eax /* store eax at the location ebx points to */
pop eax /* Update eax to new task */

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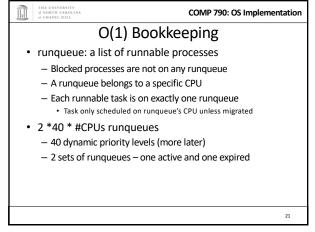


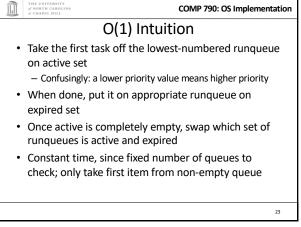
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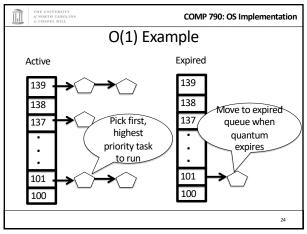
O(1) scheduler

• Goal: decide who to run next, independent of number of processes in system

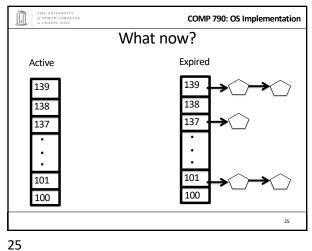
- Still maintain ability to prioritize tasks, handle partially unused quanta, etc

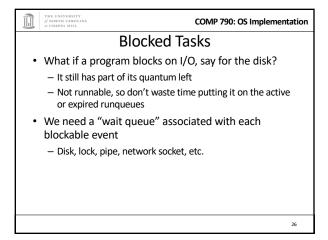




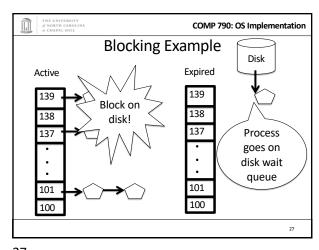


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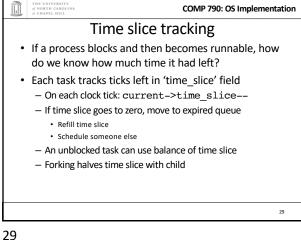


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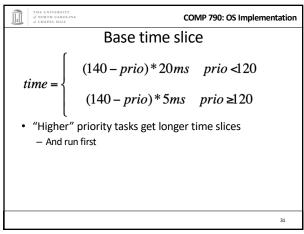
COMP 790: OS Implementation Blocked Tasks, cont. • A blocked task is moved to a wait queue until the expected event happens - No longer on any active or expired queue! · Disk example: - After I/O completes, interrupt handler moves task back to active runqueue

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COMP 790: OS Implementation More on priorities • 100 = highest priority • 139 = lowest priority • 120 = base priority - "nice" value: user-specified adjustment to base priority - Selfish (not nice) = -20 (I want to go first) - Really nice = +19 (I will go last)

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Goal: Responsive UIs

• Most GUI programs are I/O bound on the user

- Unlikely to use entire time slice

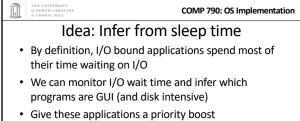
• Users get annoyed when they type a key and it takes a long time to appear

• Idea: give UI programs a priority boost

- Go to front of line, run briefly, block on I/O again

• Which ones are the UI programs?

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Give these applications a priority boost
 Note that this behavior can be dynamic

 Ex: GUI configures DVD ripping, then it is CPU-bound
 Scheduling should match program phases

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Dynamic priority

dynamic priority = max (100, min (static priority – bonus + 5, 139))

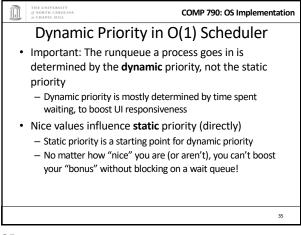
Bonus is calculated based on sleep time

Dynamic priority determines a tasks' runqueue

This is a heuristic to balance competing goals of CPU throughput and latency in dealing with infrequent I/O

May not be optimal

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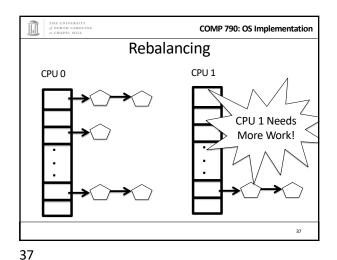
Rebalancing tasks

• As described, once a task ends up in one CPU's runqueue, it stays on that CPU forever

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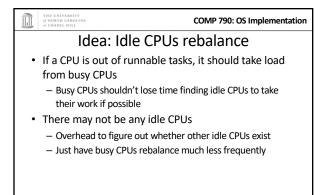
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COMP 790: OS Implementation Rebalancing tasks • As described, once a task ends up in one CPU's runqueue, it stays on that CPU forever • What if all the processes on CPU 0 exit, and all of the processes on CPU 1 fork more children? · We need to periodically rebalance · Balance overheads against benefits - Figuring out where to move tasks isn't free

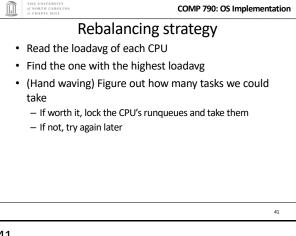
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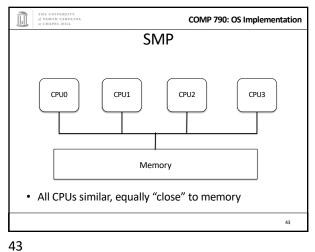
COMP 790: OS Implementation Average load • How do we measure how busy a CPU is? • Average number of runnable tasks over time · Available in /proc/loadavg

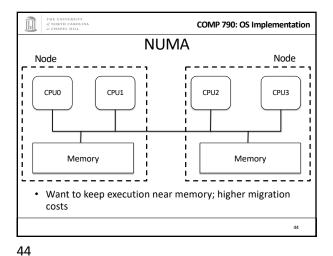
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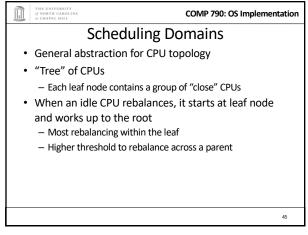


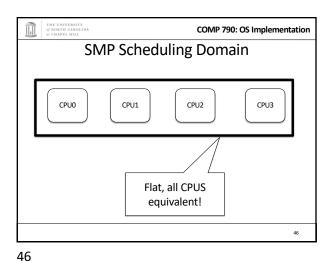
COMP 790: OS Implementation Why not rebalance? · Intuition: If things run slower on another CPU · Why might this happen? - NUMA (Non-Uniform Memory Access) - Hyper-threading - Multi-core cache behavior • Vs: Symmetric Multi-Processor (SMP) – performance on all CPUs is basically the same

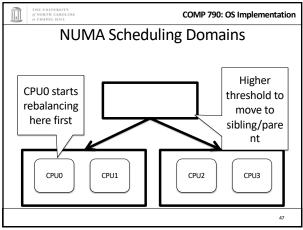
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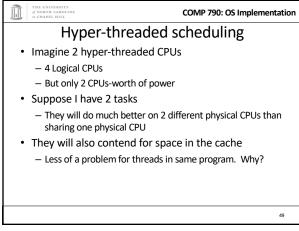






COMP 790: OS Implementation Hyper-threading · Precursor to multi-core - A few more transistors than Intel knew what to do with, but not enough to build a second core on a chip yet • Duplicate architectural state (registers, etc), but not execution resources (ALU, floating point, etc) • OS view: 2 logical CPUs • CPU: pipeline bubble in one "CPU" can be filled with operations from another; yielding higher utilization

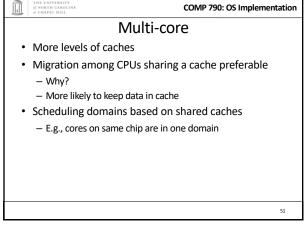
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COMP 790: OS Implementation NUMA + Hyperthreading Domains Physical Logical CPU CPU NUMA DOMAIN 1 is a sched domain CPU0 CPU2 CPU4 CPU6 CPU1 CPU5 CPU3 CPU7

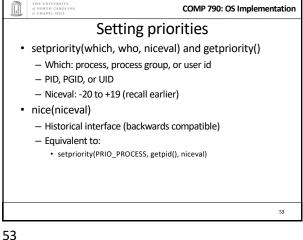
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COMP 790: OS Implementation Outline · Policy goals · Low-level mechanisms O(1) Scheduler · CPU topologies · Scheduling interfaces

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THE UNIVERSITY
of NORTH CAROLINA
at CHAPEL HILL COMP 790: OS Implementation **Scheduler Affinity** · sched_setaffinity and sched_getaffinity • Can specify a bitmap of CPUs on which this can be scheduled - Better not be 0! · Useful for benchmarking: ensure each thread on a dedicated CPU

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