On the Theory of Stochastic Processors

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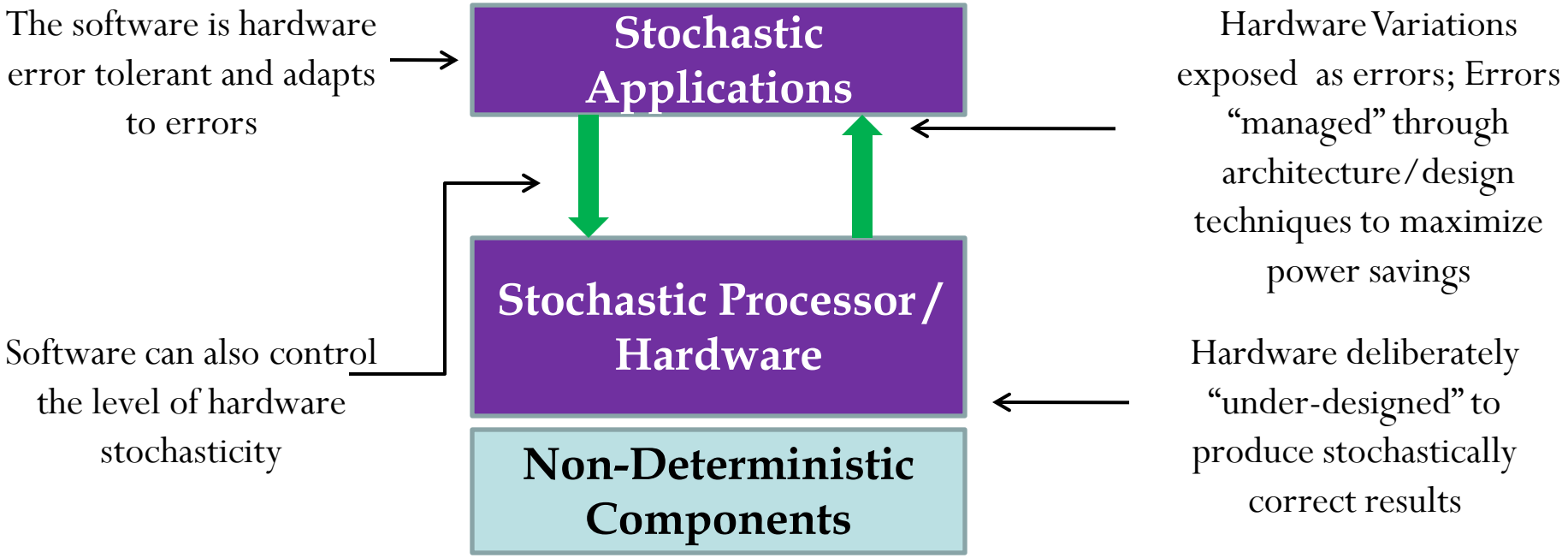
Motivation

- Exponential decrease in the size of transistor - **Moore's Law**
- Difficult to make small transistors reliable
- Manufacturing variations and workload/ environmental variations increase
- Design overhead increases
- Increase in the overall cost

Status quo cannot continue:
Need to find a solution to the uncertainties in a chip

Research Vision: Computing with Stochastic Processors

- Fundamentally Rethink the Correctness Contract between Hardware and Software



The goal of our research is to explore approaches to architect and design stochastic processors and stochastic applications.

Outline

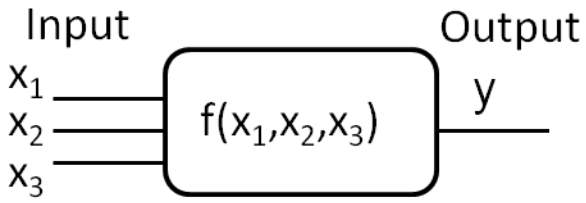
- First formal model stochastic circuits (processors)
- Define measure of correctness of stochastic circuits *(Correctness Factor)*
- Analysis of correctness factor for simple circuits

Semantics of Stochastic Devices and Circuits

The Model

Stochasticity in a device

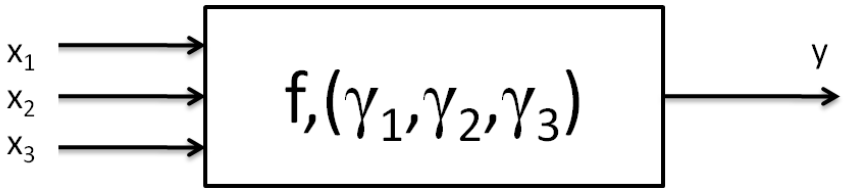
- Delay in process an input
- Processing the input values
- Output of a device

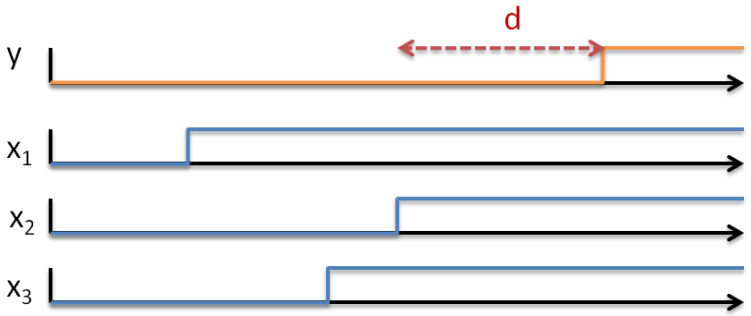


Stochasticity of interest : Random delay associated with each input

Stochastic Device

- For 'N' inputs, at each cycle, a delay is associated with the corresponding input value
- Delays generated from a delay distribution





- A stochastic device can be precisely specified
  - Device function f : $\{0,1\}^N \rightarrow \{0,1\}$
  - Discrete Delay Distributions $\gamma_1, \ldots, \gamma_N$

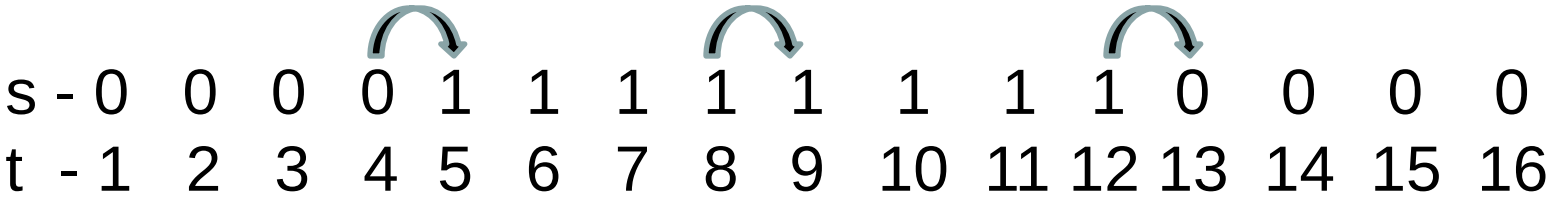
Input sources

- Model the inputs to a stochastic circuit as sources
- *K*-periodic source is an entity that produces 1-bit output that may change every K cycles.

$$s(t) = \begin{cases} 1 \text{ with probability } p \\ 0 \text{ with probability } 1\text{-}p \end{cases} \quad \text{when } t = vK$$

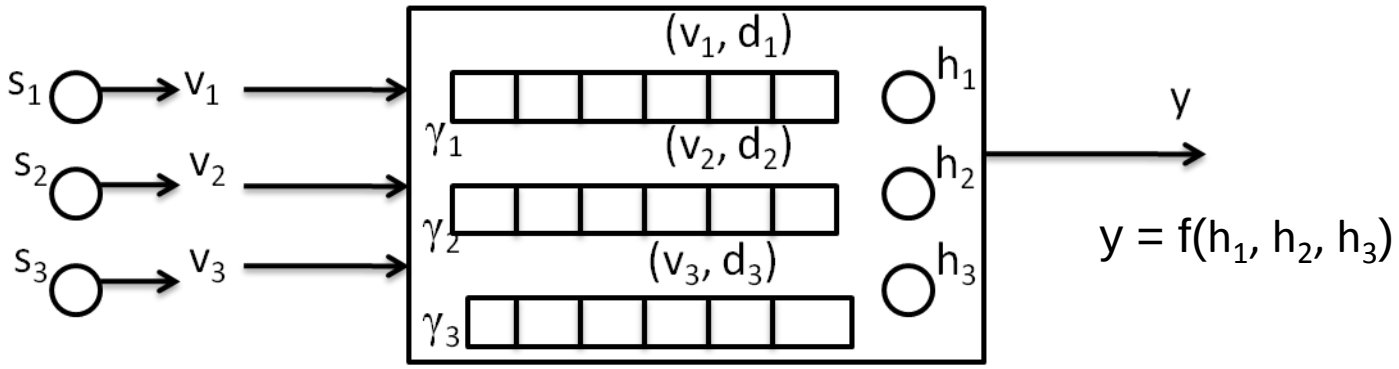
$$s(t) = s(vK) \quad \text{when } vK < t < (v+1)K$$

source with period 4 and parameter 0.5



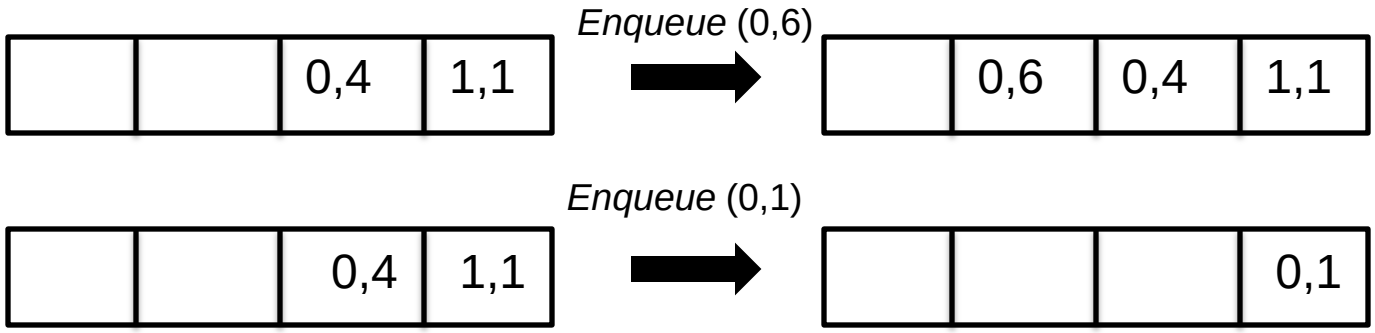
Semantics of a Device

- For each input x_i , for every input cycle, a delay *d* is associated with it
- State of a device is a collection of queues, each queue stores the inputs yet to be processed
- Queue outputs (Hidden)



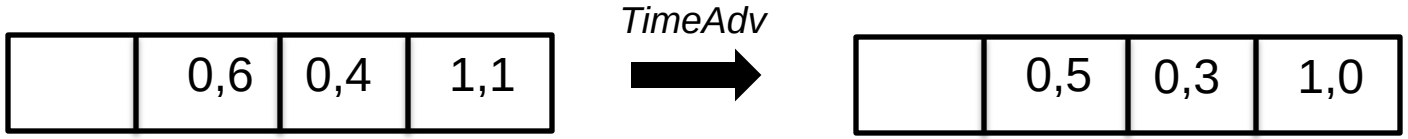
Semantics of a stochastic device

- *Enqueue* : Insert (v_i, d_i) into $queue_i$ and remove all (v,d) from it, where $d \leq d_i$

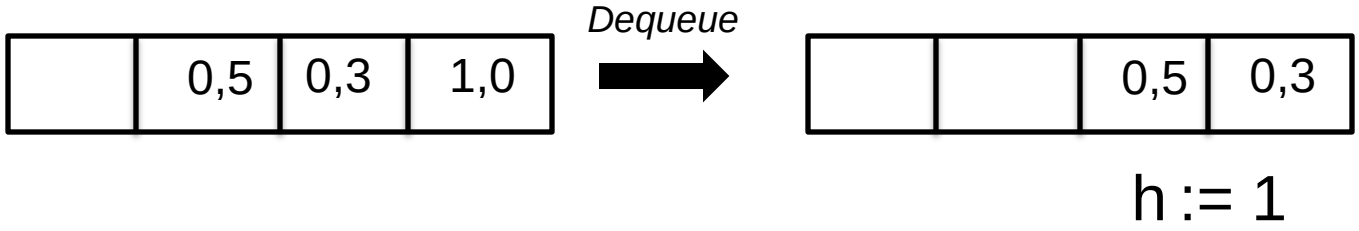


Enqueue drops the elements with larger delay, the device is different from standard FIFO queues

- *TimeAdv* : for all (v_i, d_i) in $queue_i$, $d_i = d_i - 1$;



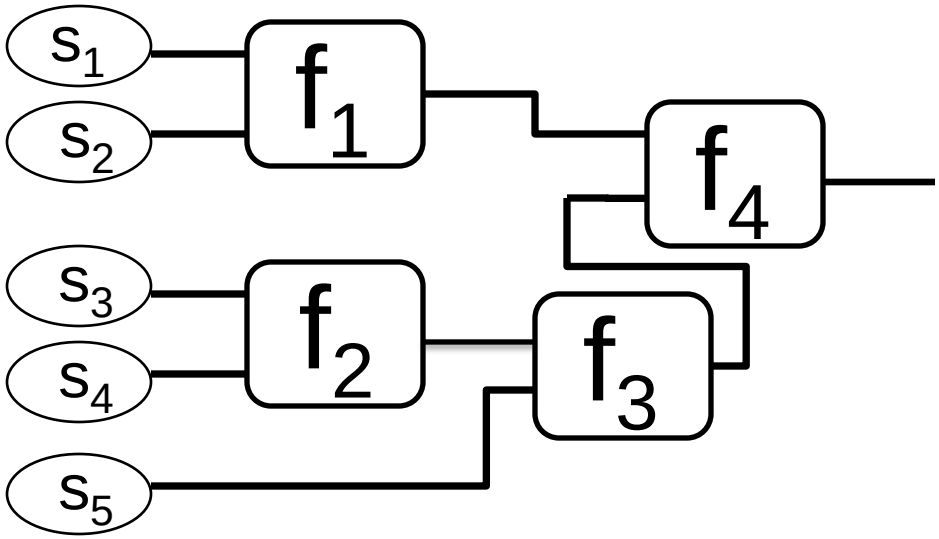
- *Dequeue* : if $(v_i, 0)$ in $queue_i$, $h_i := v_i$; $y := f(h_1, \ldots, h_n)$



Lemma: A stochastic device is a Markov chain

Stochastic Circuits

- Interconnection of sources and devices.
- Stochastic feed-forward circuit (no feedback loops)

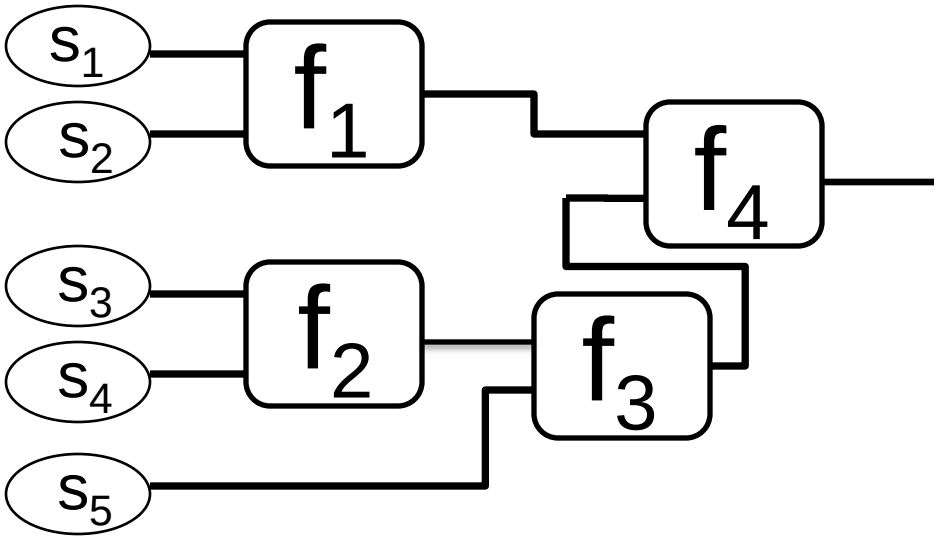


$$f_C = f_4(f_1(s_1,s_2),f_3(f_2(s_3,s_4),s_5))$$

- Depth of the circuit = 3

Circuit Function

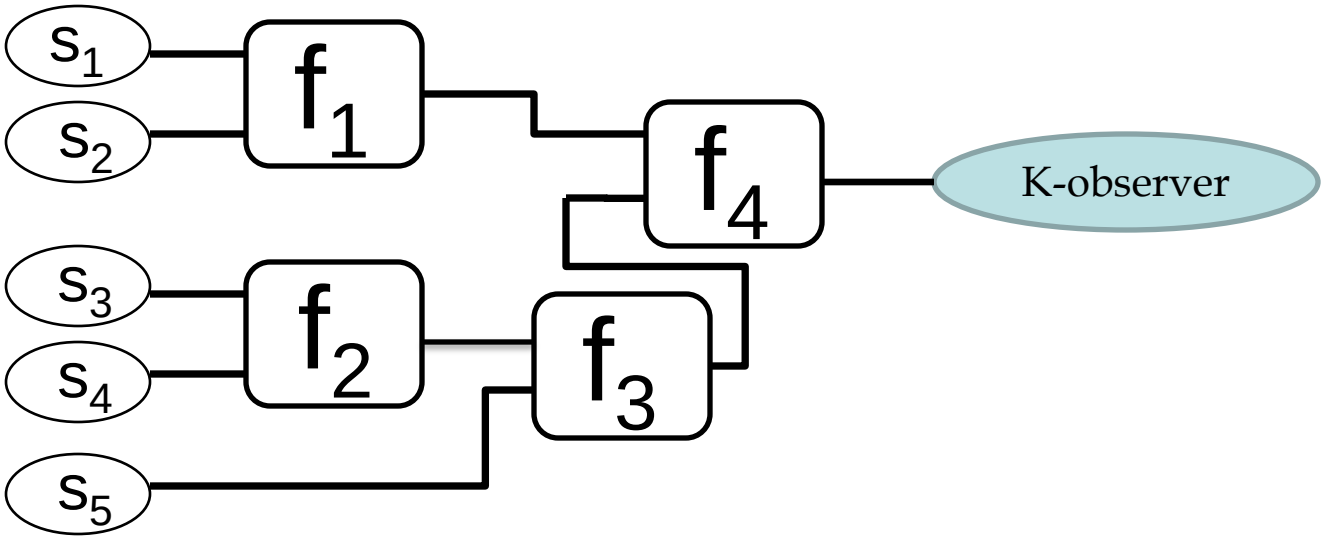
- The same inputs are given *long enough* the output will *stablize* to $f_c(a,b,c,d,e)$
- Suppose $\max(\gamma_i) = R$, let $K > 3R$, then for K-sources every input produces a correct output



But, we want to observe the outputs a faster rate!

Correctness of a stochastic circuit

- Correctness is defined w.r.t an observation period, say K
- The output is correct if at t, iff $y(t) = f_c(s_1(t-K), \ldots, s_m(t-K))$
- Let Z be a variable where
  $Z(t) = Z(t-1) + 1$ if t = vK and the output is *correct*
  $= Z(t-1)$ otherwise
- Correctness factor of circuit with observation period K is the fraction of correct outputs in the long run
  $CF_K = Lim_{t\to\infty} Z(t)/(t/K)$



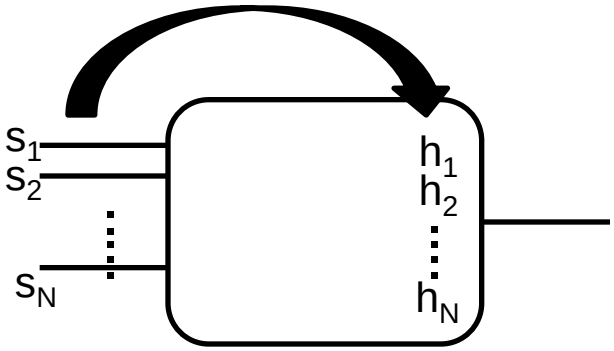
Analytical expression for evaluation of correctness factor

Analysis of CF

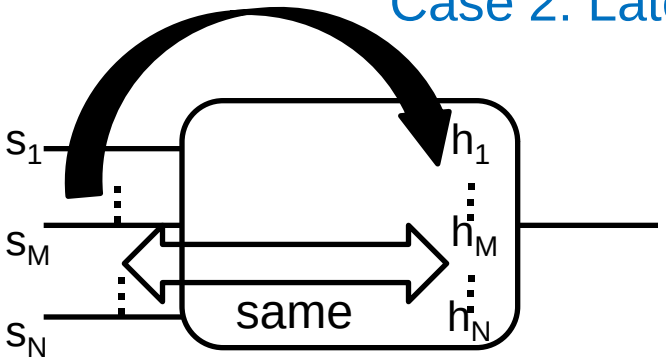
Analytical Expressions for CF_K for a Circuit with a single device

Three cases for having a correct output

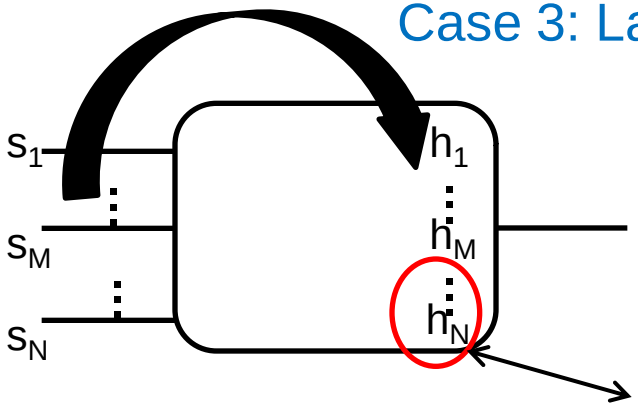
Case 1 : Timely



Case 2: Late but lucky



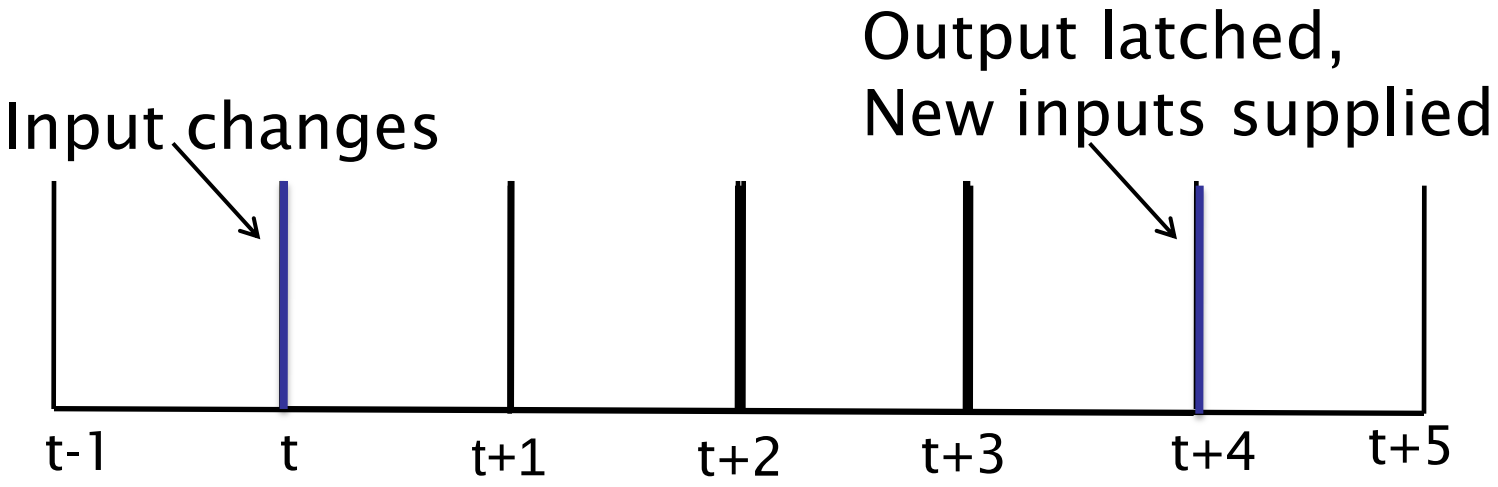
Case 3: Late but lucky



Never mind, the output is the same

Timely Arrival Probability E(γ,K)

- The probability that at least one of the previous K inputs will be latched properly
- For example, Period K = 4;

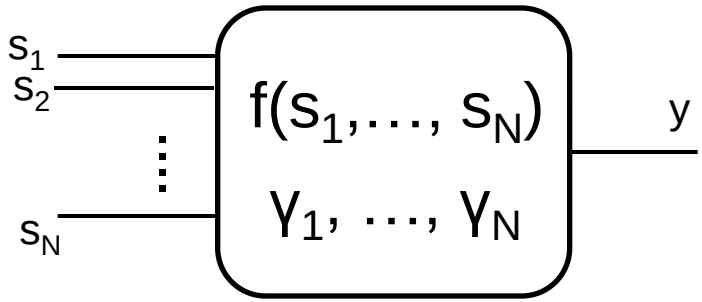


E(γ,4) represents the probability that at least one of the inputs at t, t+1, t+2, t+3 are latched at t+4

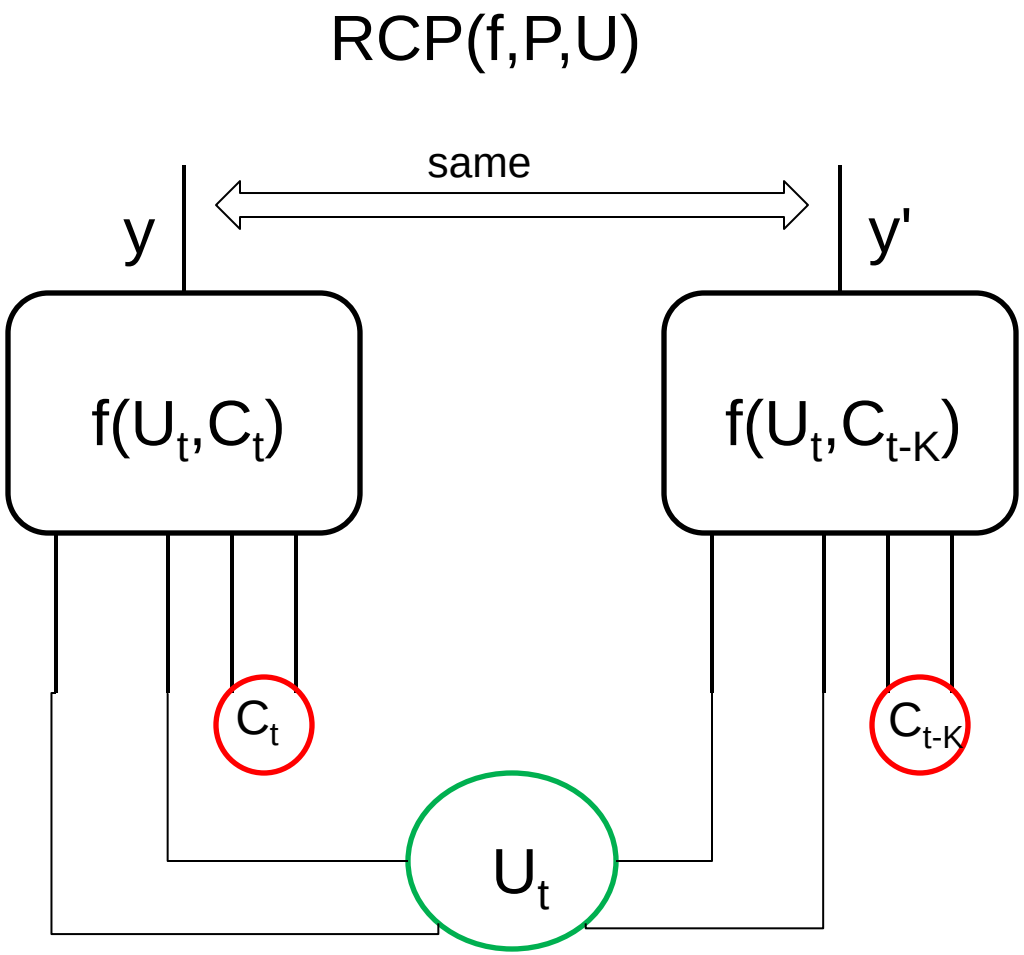
Properties of E(γ,K)

- Depends only on γ and K
- Closed form expression for

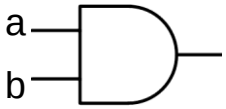
$$E(\gamma,K) = 1 - \prod_{i=1}^{K-1} \Gamma(> i)$$

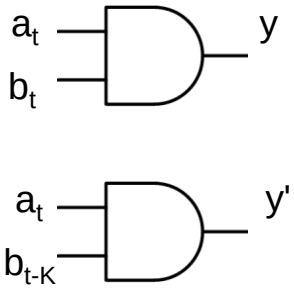


Late but Lucky : Random Correctness Probability (RCP)



Example : RCP(And,{0.5,0.5},U)





U = {a}

if $a_t = 1$, $f(a_t,b_t) = f(a_t,b_{t-K})$ only if $b_t = b_{t-K}$

Probability = $0.5 \times (0.5 \times 0.5 + 0.5 \times 0.5) = 0.25$

reminds of Case 2 late but lucky?

if $a_t = 0$, $f(a_t,b_t) = f(a_t,b_{t-K})$ - Probability = 0.5

reminds of case 3 late by lucky ?

RCP(And,{0.5,0.5},{a}) = 0.75

RCP of various devices

	2 sources .5, .5		
	C = {a}	C = {b}	C = {a,b}
Const. 0	1	1	1
AND	¾	¾	5/8
OR	¾	¾	5/8
XOR	½	½	½
NAND	¾	¾	5/8
NOR	¾	¾	5/8
NXOR	½	½	½

RCP of various devices

	2 sources .5, .5			2 sources .9, .1		
	C = {a}	C = {b}	C = {a,b}	C = {a}	C = {b}	C = {a,b}
Const. 0	1	1	1	1	1	1
AND	¾	¾	5/8	.838	.982	.8362
OR	¾	¾	5/8	.982	.838	.8362
XOR	½	½	½	.82	.82	.7048
NAND	¾	¾	5/8	.838	.982	.8362
NOR	¾	¾	5/8	.982	.838	.8362
NXOR	½	½	½	.82	.82	.7048

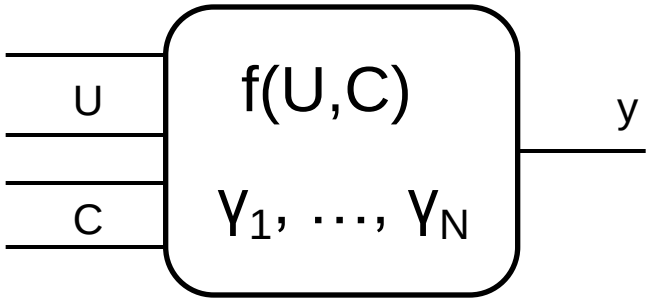
Expression for CF_K

- Consider only a subset U = { j_1,…, j_n} of inputs
- Probability of *correctness given timely bits in U* =

$$\prod_{i \in U} E(\gamma_i, K) * \prod_{j \in I/U} (1 - E(\gamma_j, K)) * RCP(f, P, U)$$

Probability that U inputs will latch

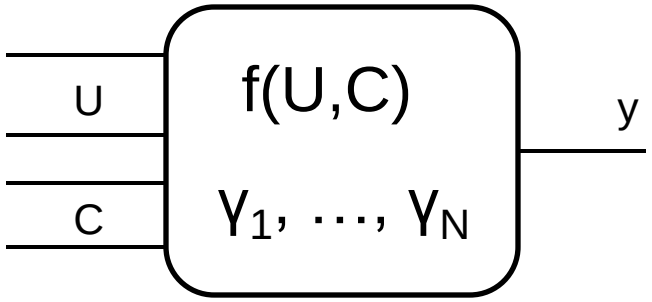
Probability of output being correct



Expression for CF_K

- Summing over all subsets U

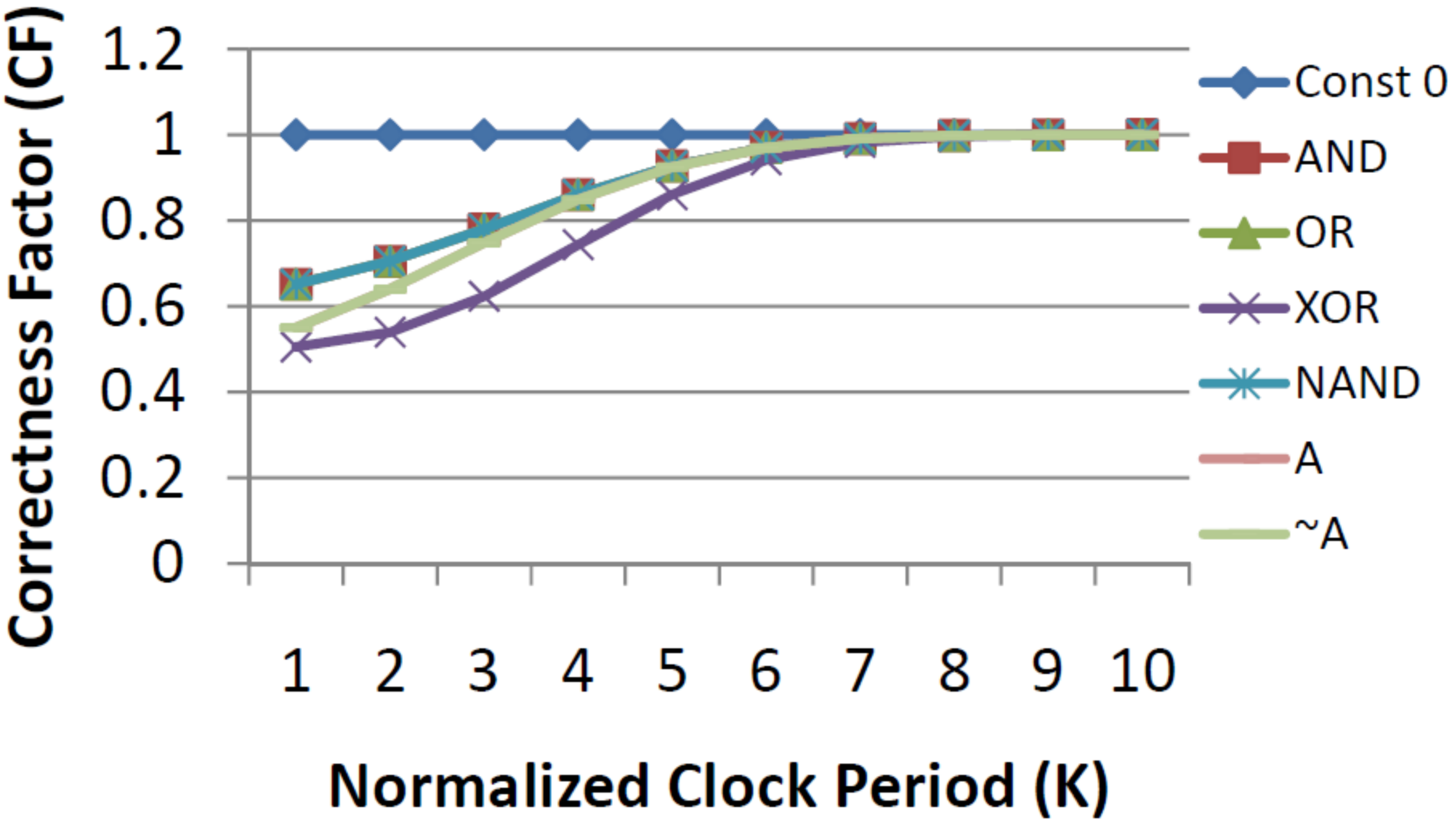
$$CF_K = \sum_{\forall U} \left(\prod_{i \in U} E(\gamma_i, K) * \prod_{j \in I/U} (1 - E(\gamma_j, K)) * RCP(f, P, U) \right)$$



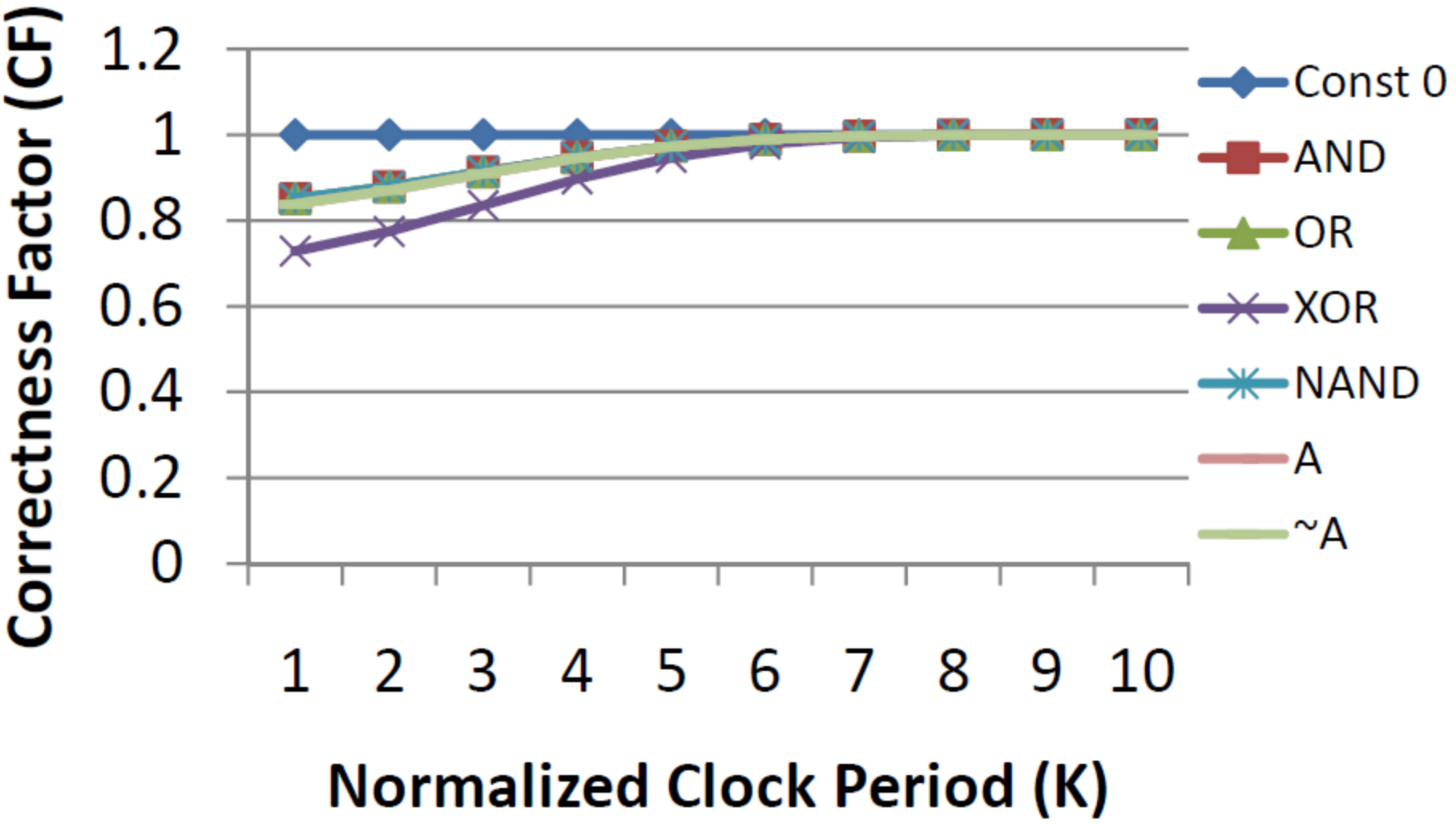
Correctness Factors for various Stochastic Devices and Sources

- Analytical results for correctness factor for various stochastic devices
  - 2 bit devices AND, OR, XOR, etc.
  - Uniform and Poisson like distribution for delays, range within 10
  - 2 types of source setting (0.5,0.5) and (0.9, 0.1)
  - Vary observation period K (and hence the source clock period)

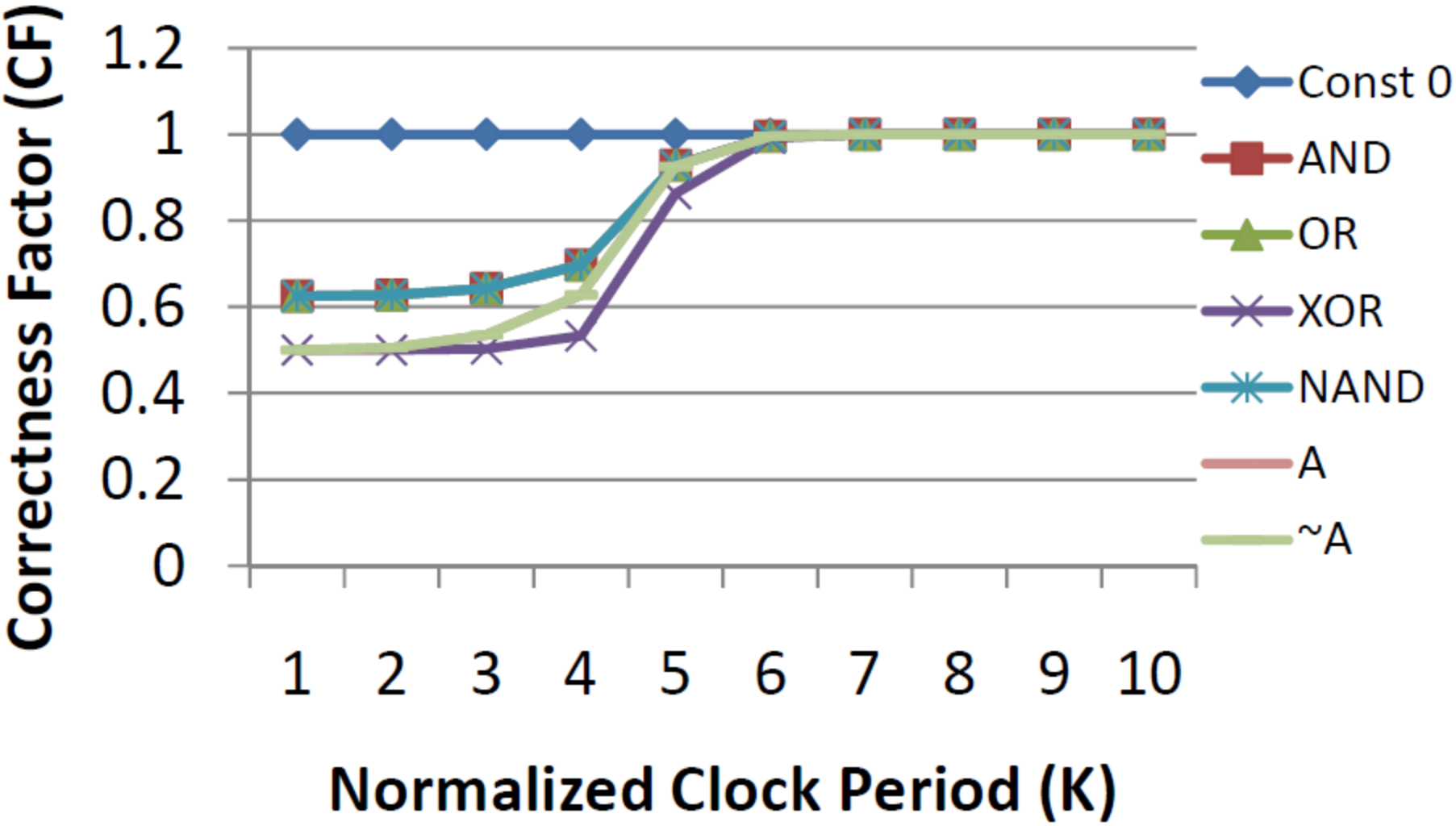
Uniform delay distribution with random sources of parameters (0.5, 0.5)



Uniform delay distribution with random sources of parameters (0.9, 0.1)



Poisson delay distribution with random sources of parameters (0.5, 0.5)



Conclusion

- Model for stochastic devices and circuits and definition of stochastic correctness in terms of long term behavior
- Analysis of correctness for a class of elementary circuits of depth 1 and 2
- Model checking (PRISM) and simulations have been used to validate the analysis
- **Comment:** The theory applies to other settings where the inputs affect the outputs with stochastic delays
- **Future directions:**
  - Compositional analysis of more complex circuits
  - Lower bounds on the limits of stochastic computation with power constraints

Thank you!