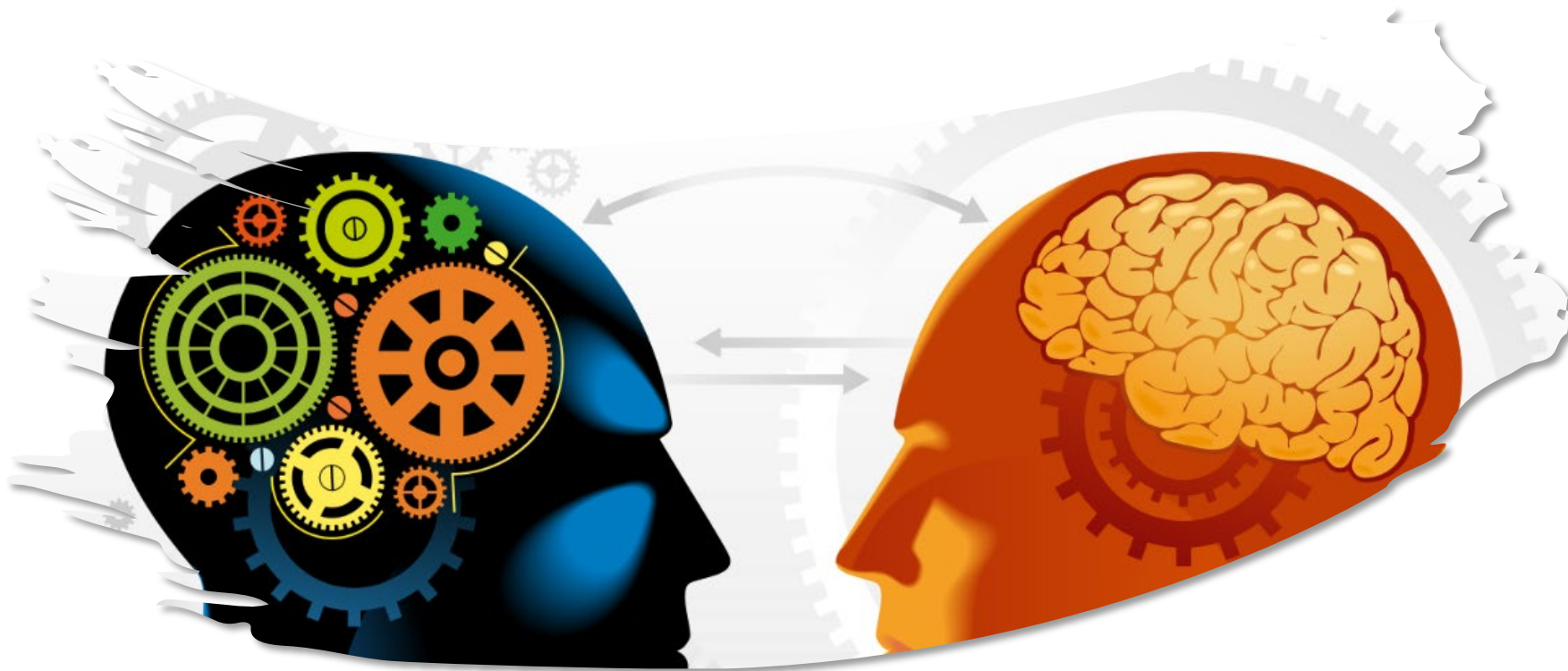




Building the Infinite Brain

COMP 690 (193)

Raghavendra Pradyumna Pothukuchi



THE UNIVERSITY
of NORTH CAROLINA
at CHAPEL HILL

✉ raghav@cs.unc.edu

Writing the Project Proposal



The Heilmeier Catechism

<https://www.darpa.mil/about/heilmeier-catechism>

George H. Heilmeier, *former DARPA director*

2-page proposals due 1/21

Goal: What are you trying to do?

State of the art and challenges/limitations: How is it done today, and what are the limits of current practice?

Novelty and realizability: What is new in your approach, and why do you think it will be successful?

Significance and impact: Who cares? If you are successful, what difference will it make?

Executional challenges: What are the risks?

Effort: How much will it cost?

Timeline: How long will it take?

Metrics and deliverables: What are the midterm and final “exams” to check for success?



More on The Project

Working project

Examples

- An FPGA/microcontroller implementation of FFT and analysis of power and performance
 - Software to improve/maintain a BCI tool or other software
 - BRAND: <https://github.com/brandbci/brand>
 - Foresee: <https://github.com/bci-foresee/foresee>
 - Verification (or Correctness) specification and analysis of a BCI hardware or software kernel
 - An EEG BCI game of Pong
 - An analysis of algorithms used for seizure detection and their suitability for on-device execution
 - A compiler to translate a BCI application to fit microcontrollers
 - Python to Verilog translation for DWT in BCI processor design
 - Extension of a BCI processing architecture
 - Evaluation of a machine learning algorithm for speech decoding and suggested re-design for on-device execution
 - Leveraging neuroscientific markers for efficient movement intent decoding on device
 - An analysis of cursor movement methods identifying key computational techniques and bottlenecks
- ... (last semester project abstracts will be uploaded for reference)

You should argue for why your design (hardware, software) is good



You can search online for inspiration, but do not use someone else's code or work—recall the honor code



Suggestions on Paper Reading

Read in detail

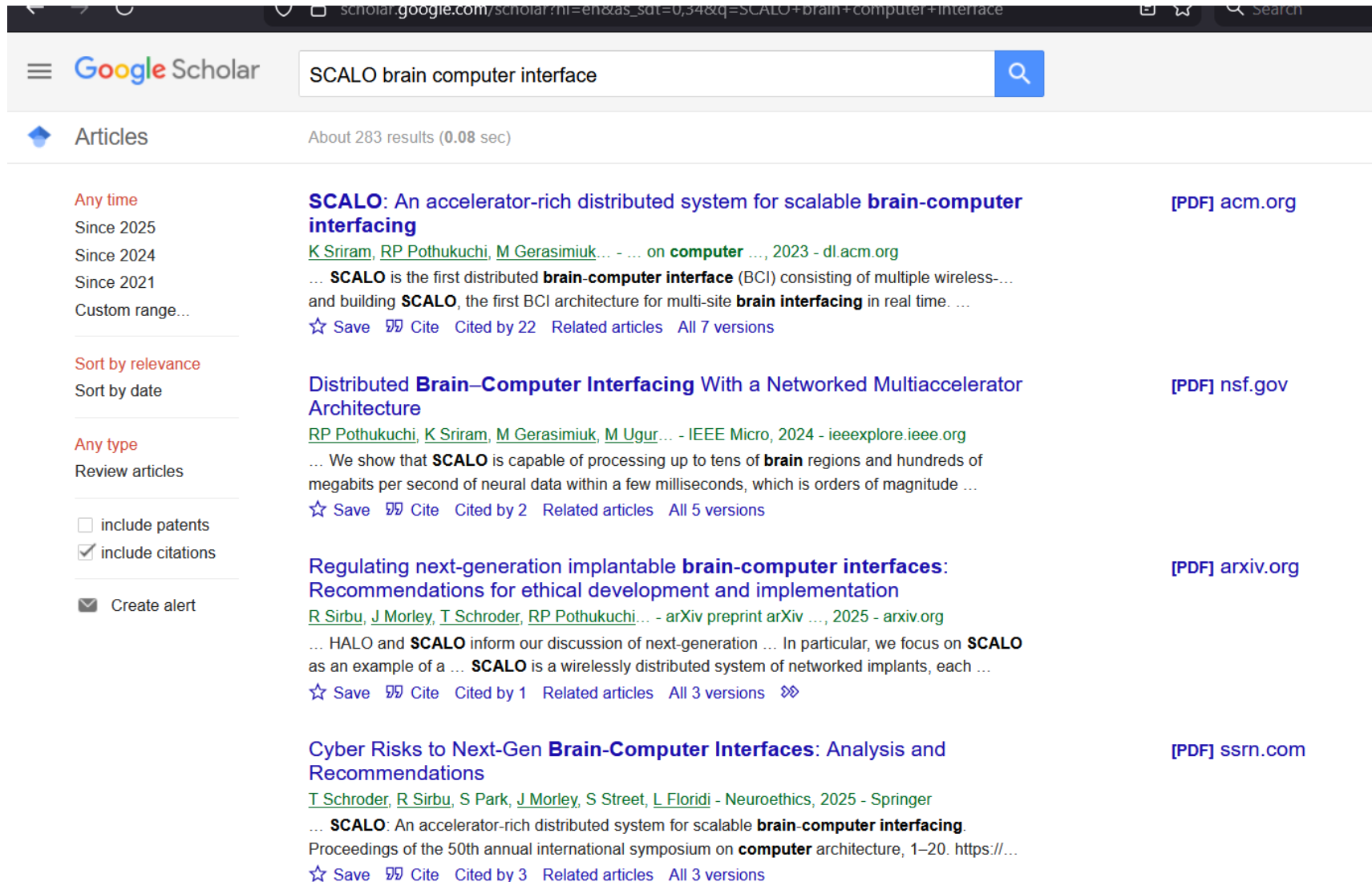
Multiple passes

Use manual search first

You'll discover many things—helps with breadth and depth



Suggestions on Paper Reading



The screenshot shows a Google Scholar search for "SCALO brain computer interface". The search bar at the top contains the text "SCALO brain computer interface" and a magnifying glass icon. Below the search bar, the results are listed under the heading "Articles". The first result is titled "SCALO: An accelerator-rich distributed system for scalable brain-computer interfacing" by K Sriram, RP Pothukuchi, and M Gerasimiuk, published in 2023 in the DL.acm.org journal. The second result is titled "Distributed Brain-Computer Interfacing With a Networked Multiaccelerator Architecture" by RP Pothukuchi, K Sriram, M Gerasimiuk, and M Ugur, published in 2024 in the IEEE Micro journal. The third result is titled "Regulating next-generation implantable brain-computer interfaces: Recommendations for ethical development and implementation" by R Sirbu, J Morley, T Schroder, and RP Pothukuchi, published in 2025 as an arXiv preprint. The fourth result is titled "Cyber Risks to Next-Gen Brain-Computer Interfaces: Analysis and Recommendations" by T Schroder, R Sirbu, S Park, J Morley, S Street, and L Floridi, published in 2025 in the Neuroethics journal. The left sidebar contains filters for "Any time", "Sort by relevance", "Any type", and checkboxes for "include patents" and "include citations".

Google Scholar

SCALO brain computer interface

Articles About 283 results (0.08 sec)

Any time
Since 2025
Since 2024
Since 2021
Custom range...

Sort by relevance
Sort by date

Any type
Review articles

☐ include patents
☒ include citations

☒ Create alert

SCALO: An accelerator-rich distributed system for scalable brain-computer interfacing [PDF] acm.org
K Sriram, RP Pothukuchi, M Gerasimiuk... - ... on computer ..., 2023 - dl.acm.org
... SCALO is the first distributed brain-computer interface (BCI) consisting of multiple wireless-... and building SCALO, the first BCI architecture for multi-site brain interfacing in real time. ...
☆ Save ⓘ Cite Cited by 22 Related articles All 7 versions

Distributed Brain-Computer Interfacing With a Networked Multiaccelerator Architecture [PDF] nsf.gov
RP Pothukuchi, K Sriram, M Gerasimiuk, M Ugur... - IEEE Micro, 2024 - ieeexplore.ieee.org
... We show that SCALO is capable of processing up to tens of brain regions and hundreds of megabits per second of neural data within a few milliseconds, which is orders of magnitude ...
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Regulating next-generation implantable brain-computer interfaces: Recommendations for ethical development and implementation [PDF] arxiv.org
R Sirbu, J Morley, T Schroder, RP Pothukuchi... - arXiv preprint arXiv ..., 2025 - arxiv.org
... HALO and SCALO inform our discussion of next-generation ... In particular, we focus on SCALO as an example of a ... SCALO is a wirelessly distributed system of networked implants, each ...
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Cyber Risks to Next-Gen Brain-Computer Interfaces: Analysis and Recommendations [PDF] ssrn.com
T Schroder, R Sirbu, S Park, J Morley, S Street, L Floridi - Neuroethics, 2025 - Springer
... SCALO: An accelerator-rich distributed system for scalable brain-computer interfacing. Proceedings of the 50th annual international symposium on computer architecture, 1-20. https://...
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Suggestions on Paper Reading

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Multiple passes

Use manual search first

You'll discover many things—helps with breadth and depth

Mozart: Taming taxes and composing accelerators with shared-memory

[PDF] [acm.org](#)

[V Suresh](#), [B Mishra](#), [Y Jing](#), [Z Zhu](#), [N Jin...](#) - [Proceedings of the ..., 2024](#) - [dl.acm.org](#)

... [42] propose a **brain-computer interface** (BCI) system that includes processing units for small kernels frequently used in BCI pipelines. Recent works [43, 83] also highlight the ...

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Stimulates broad domain learning, abstract reasoning, and multi-task learning



Suggestions on Presentations

Different types of presentations

Tease them (motivate the interaction), Show them (storytelling), Throw at them (detailed review)

Presentation is an aid to an immersive experience

Draw attention where you want through color, font, objects, graphics, and *absence*
Reading notes or long text stimulates reading or hearing—not listening, and not engaging



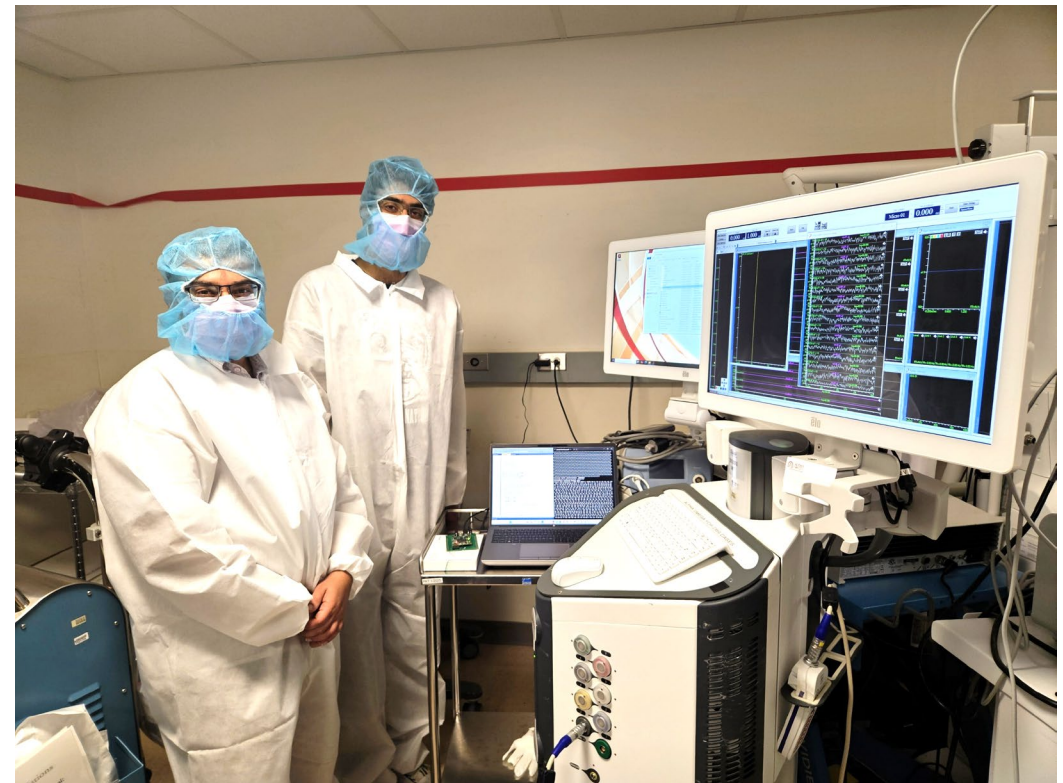
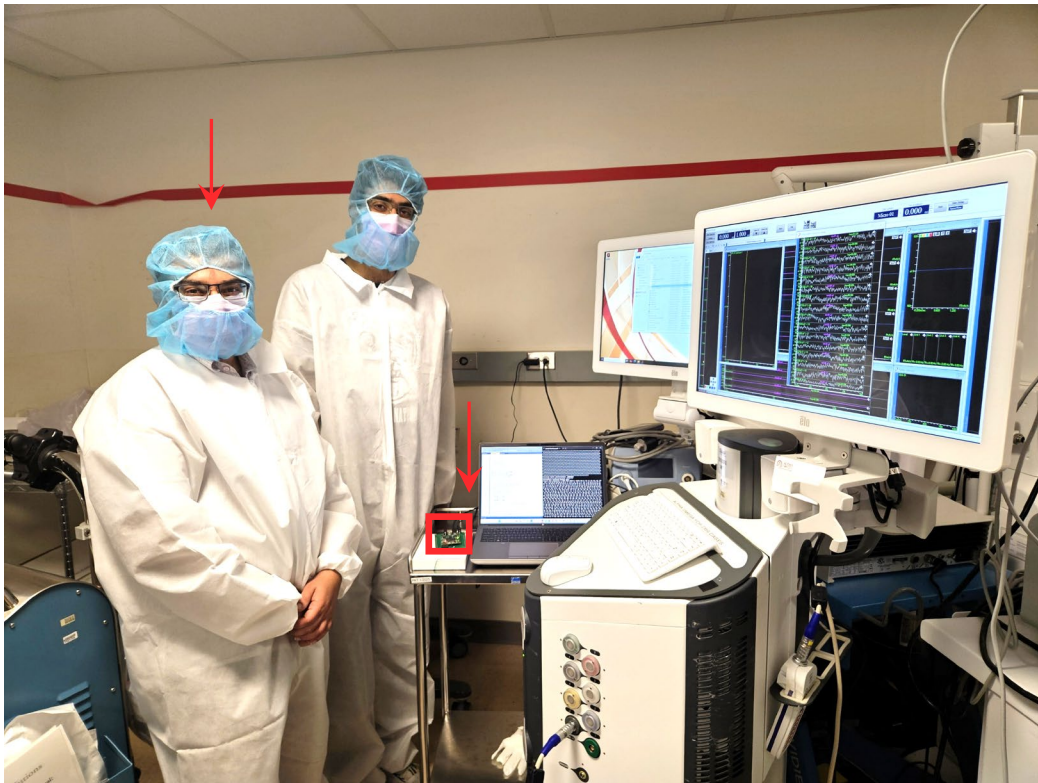
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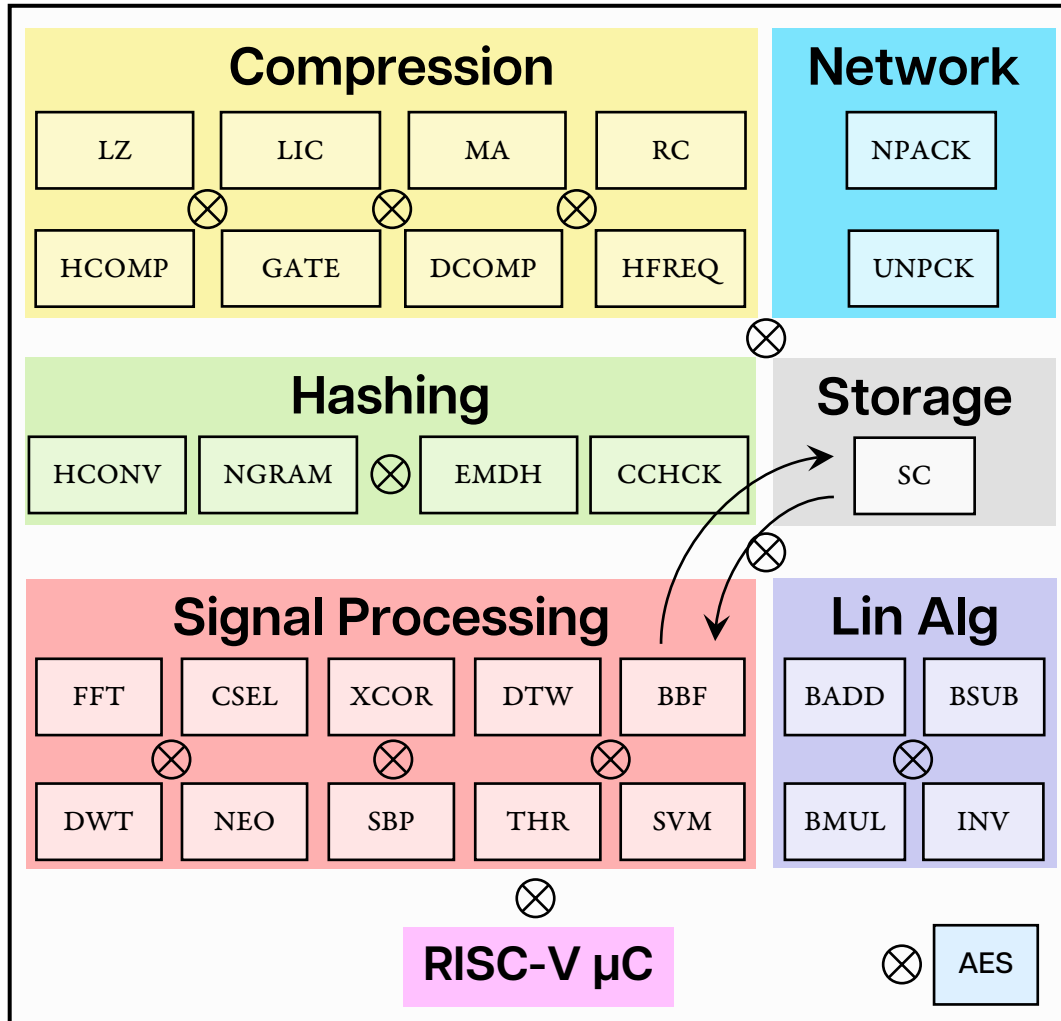
Lead the audience

Move from a high-level introduction to the nitty gritty and go back up with the wisdom

Example slide follows



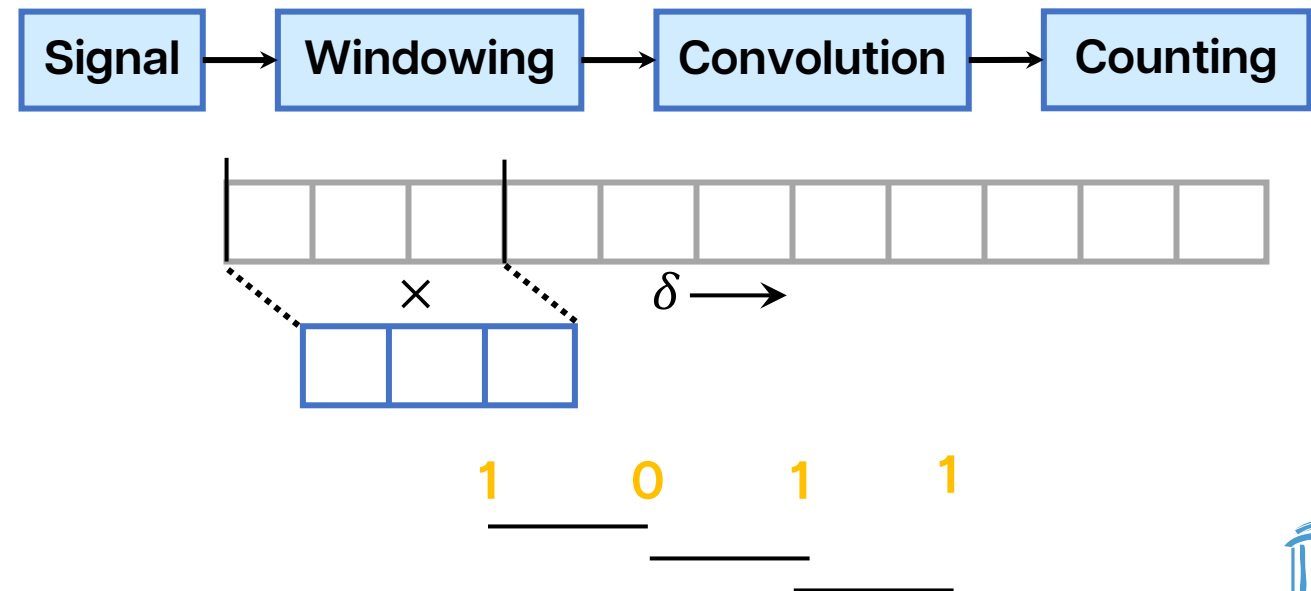
Accelerator-Rich Architecture



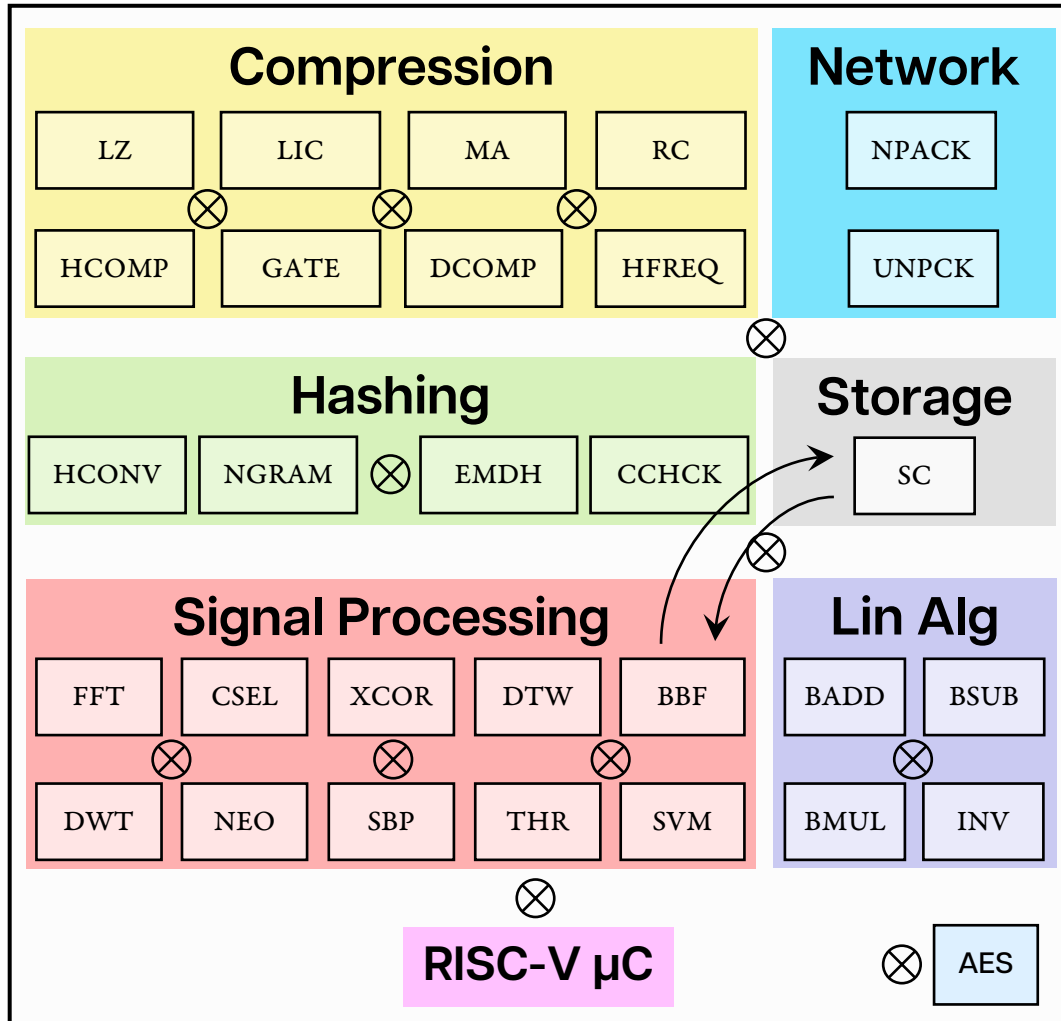
Optimize processing elements (PEs) for reuse

Locality Sensitive Hashing

Dynamic Time Warping, Euclidean Distance, Correlation, Earth-Mover's Distance



Accelerator-Rich Architecture



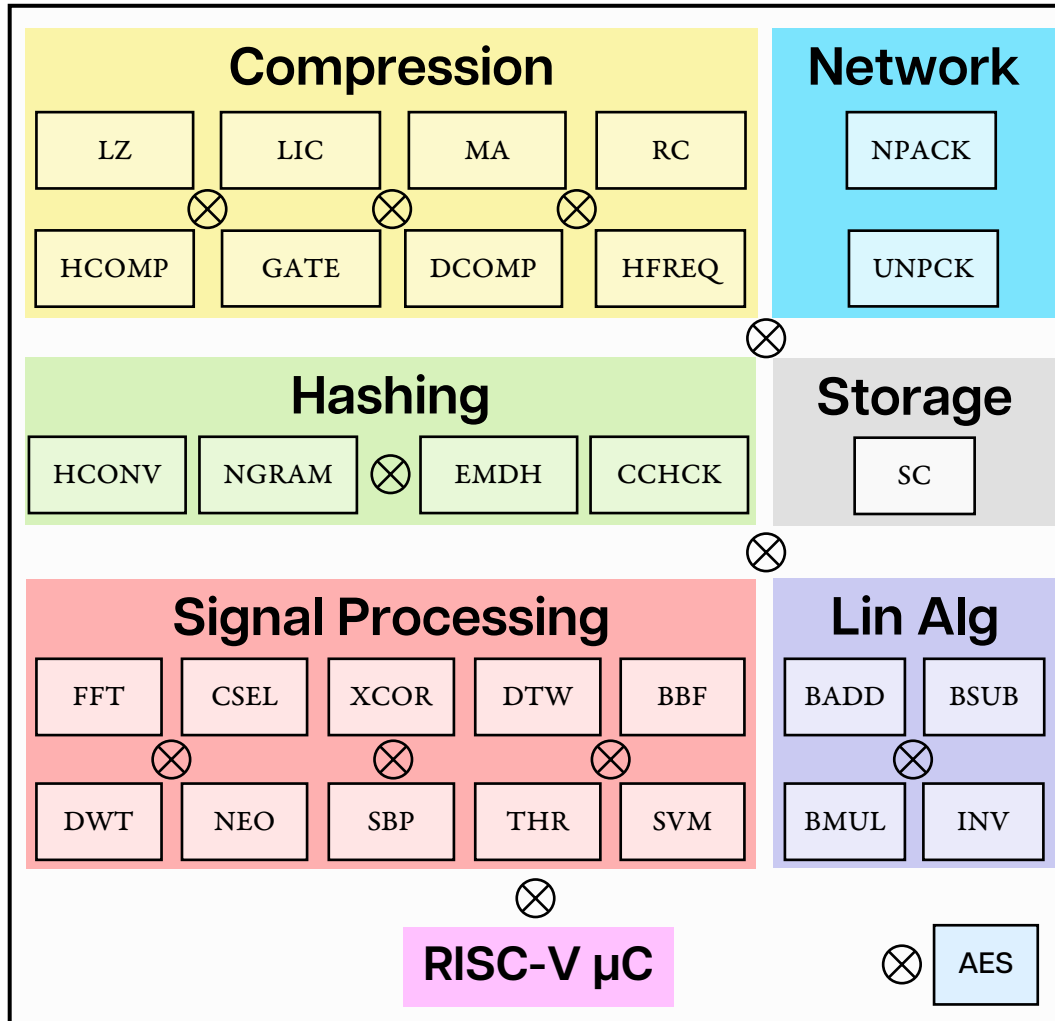
Optimize processing elements (PEs) for reuse

Per-PE clock, and frequency scaling

Configurable interconnect

Predictable power and performance

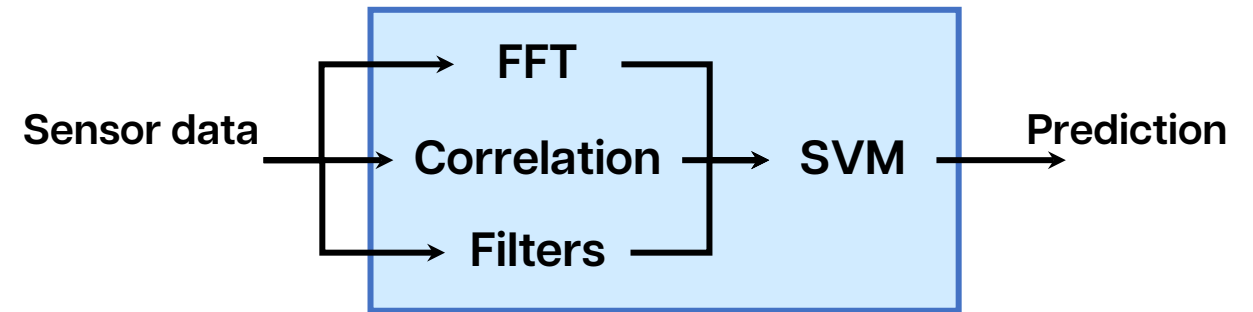
Accelerator-Rich Architecture



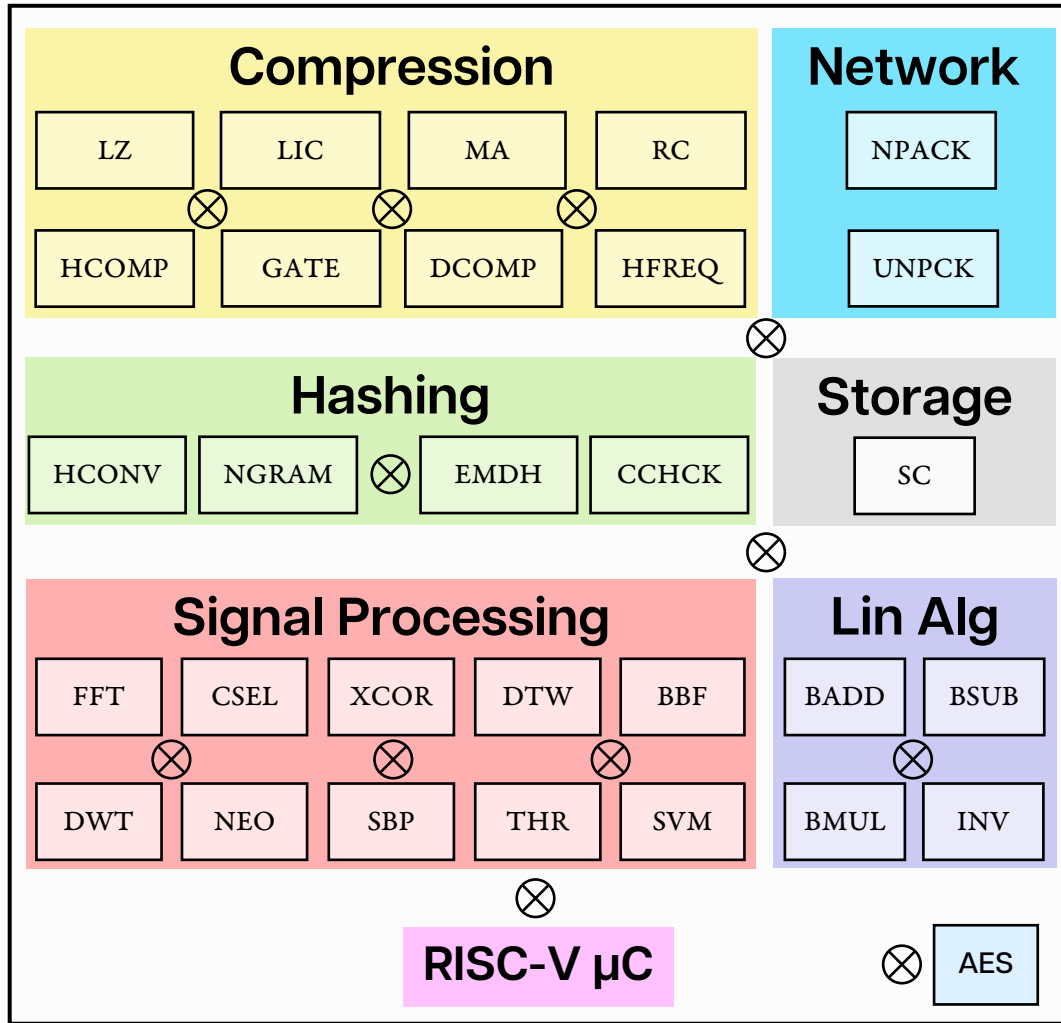
ISA, but with accelerators, for BCI applications

Accelerator as the instruction

Efficiency with flexibility



Accelerator-Rich Architecture

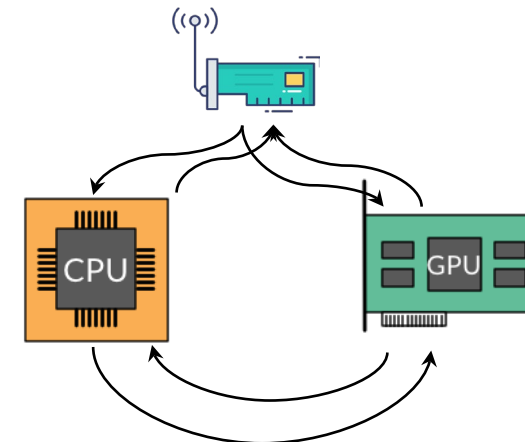


ISA, but with accelerators, for BCI applications

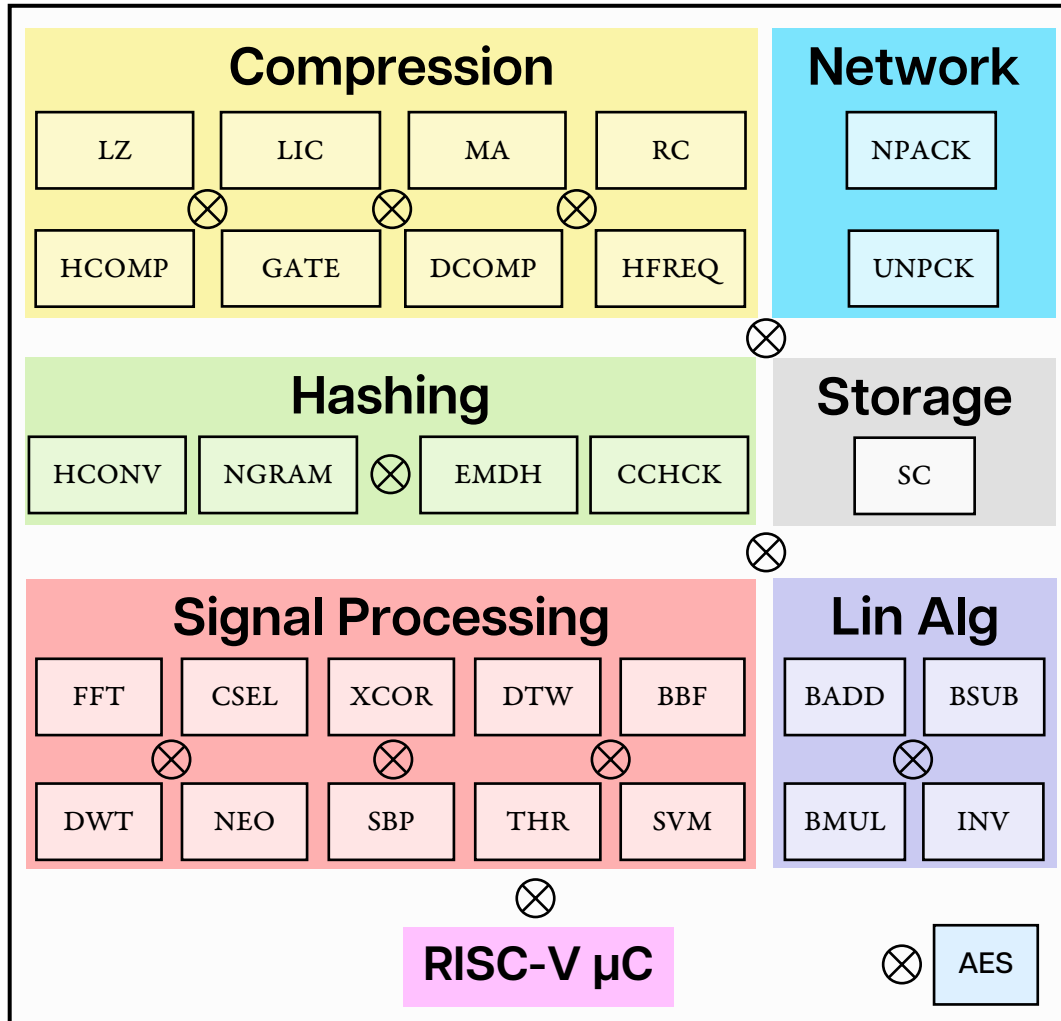
Accelerator as the instruction

Efficiency with flexibility

Minimizing CPU-led overheads



Accelerator-Rich Architecture



ISA, but with accelerators, for BCI applications

Accelerator as the instruction

Efficiency with flexibility

Minimizing CPU-led overheads

Hash-based communication for scalability

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Reading notes or long text stimulates reading or hearing—not listening, and not engaging

Lead the audience

Move from a high-level introduction to the nitty gritty and go back up with the wisdom

Make the audience think, and be excited

Show connections that weren't obvious, discuss significance, tie to real examples that matter

Practice!

Perfect practice makes perfect—to deliver the best experience



For Today

- Quick review
- **Introductions**
- **What is computer architecture?**
- **How are computer architectures analyzed and compared?**



Introductions!

Name

Grad/undergrad

Focus area

Why are you taking the course?

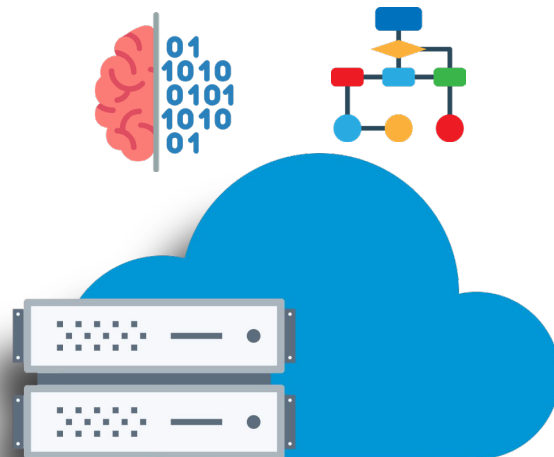


Example Application

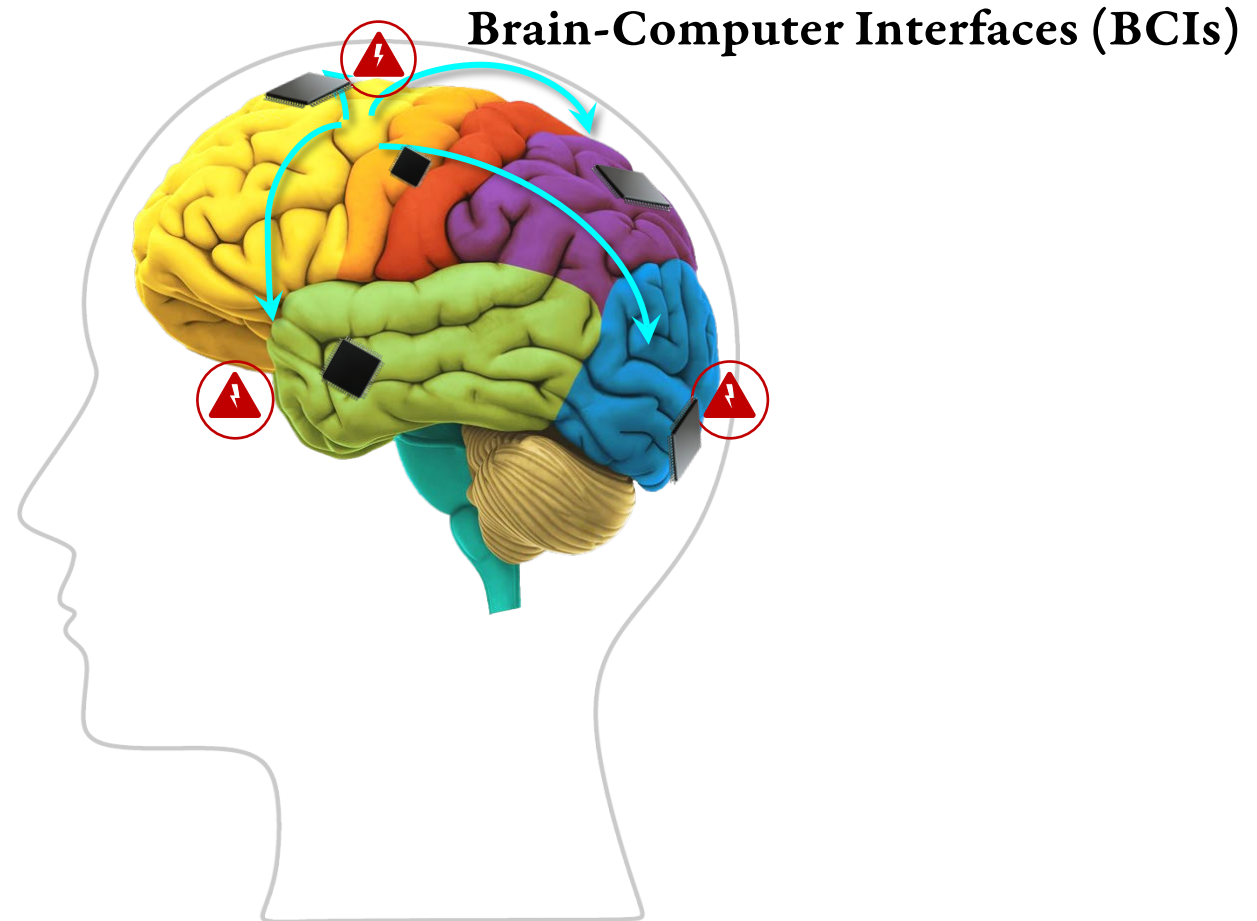
Restoring function



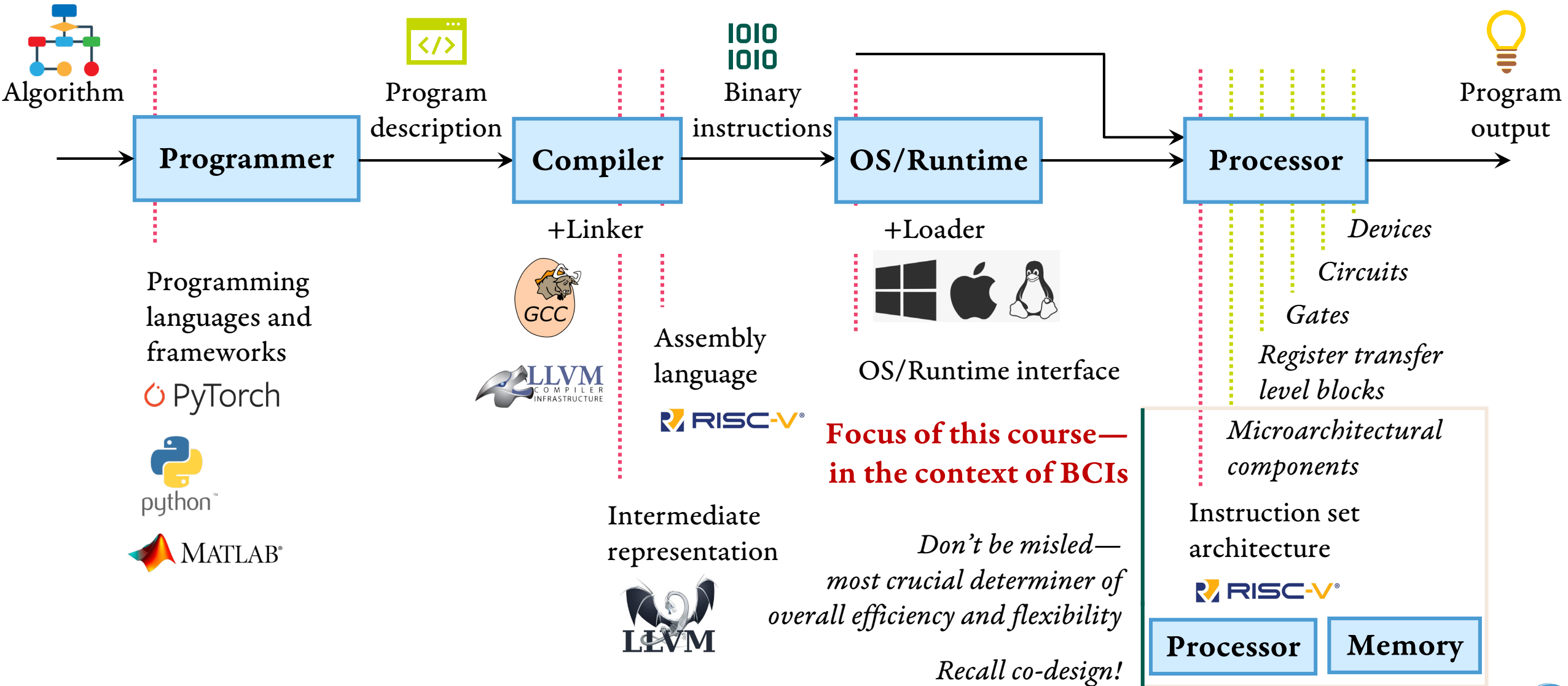
Computational cognitive
frameworks



Mitigating seizures



BCI Computing is a Full Stack Problem



What is Computer Architecture?

Previously, it meant the ISA

Most are register based (operands and results in registers), other variants include stack, accumulator

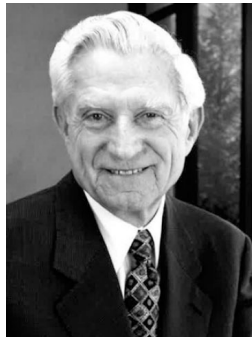
Now, it could mean everything between the OS and circuit design!

Distinctions are made based on the context

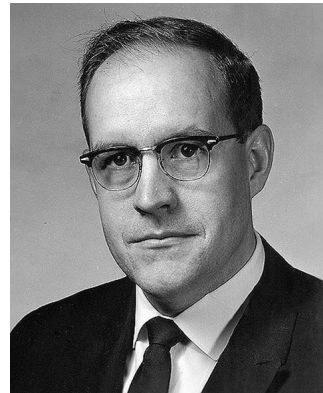
What we discuss is also called computer organization



Gerrit A. Blaauw



Gene Amdahl



Fred Brooks Jr

“The term architecture is used here to describe the attributes of a system as seen by the programmer, i.e., the conceptual structure and functional behavior, as distinct from the organization of the data flow and controls, the logical design, and the physical implementation.”

Architecture of the IBM System/360, Apr 1964

Goals of A Computer Architect



Reading task: “Hints and Principles for Computer System Design (2021)”
<https://arxiv.org/abs/2011.02455>

STEADY by AID with ART

Butler Lampson, *Pioneer in computer system design*

Applicable for BCI computers too!

Simple	Timely	Efficient	Adaptable	Dependable	Yummy	Goals
Is it clean?	Is it ready?	Is it fast?	Can it evolve?	Does it work?	Will it sell?	

Approximate	Incremental	Divide and conquer	Techniques
Speculate, compress...	Independent, iterate...	Abstractions, concurrent...	

Architecture	Automate	Review	Techniques	Test	Process
---------------------	-----------------	---------------	-------------------	-------------	---------

What?	Goals	STEADY	— Simple, Timely, Efficient, Adaptable, Dependable, Yummy
How?	Techniques	by AID	— Approximate, Incremental, Divide & Conquer
When, who?	Process	with ART	— Architecture, Automate, Review, Techniques, Test



Measuring Goals

Simple

Timely

Efficient

Adaptable

Dependable

Yummy

Time-to-market

Latency

Uptime

Throughput

Downtime

Energy

Mean time to failure

Throughput per watt

Mean time between failures

Energy per bit

Power

Energy×Delay (ED or EDP)

Quality of service

Tail latency



Measuring Execution Time

$$\text{Execution time} = \frac{\text{instructions}}{\text{program}} \times \frac{\text{cycles}}{\text{instruction}} \times \frac{\text{time}}{\text{cycle}}$$

Path length *CPI* $\left(= \frac{1}{IPC}\right)$ *period* $\left(= \frac{1}{f}\right)$



Measuring Power

$$\text{Power} = \text{Power}_{\text{static}} + \text{Power}_{\text{dynamic}}$$

$$\text{Power}_{\text{dynamic}} \propto \text{Activity} \times \text{Capacitance} \times \text{Voltage}^2 \times \text{frequency}$$

$$\text{Power}_{\text{static}} \propto \text{Voltage} \times \text{Current}$$



Improving Efficiency

First get it right, and then, get it fast

Efficiency of resources—what are they?

Computing, storage, communication, power, energy

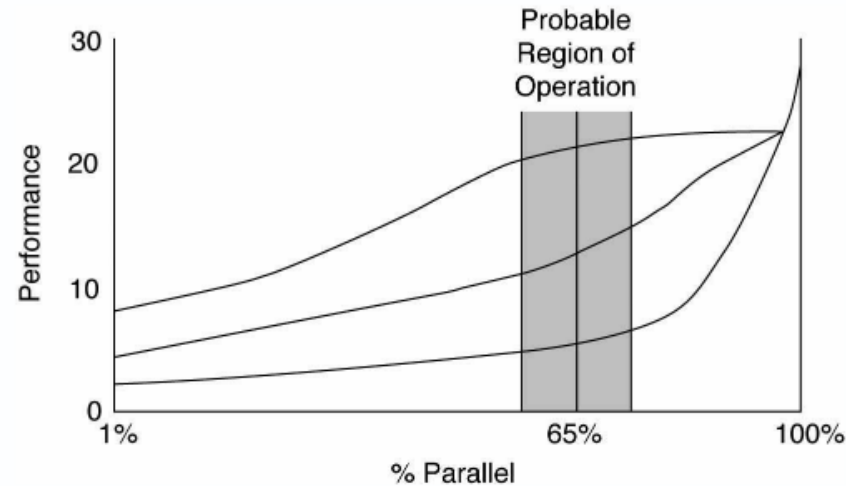
Concept of a bottleneck

The part of the system that consumes the most resources

E.g., single server under contention, sequential execution, administration



Amdahl's Law



“Validity of the Single Processor Approach to Achieving Large Scale Computing Capabilities”, AFIPS 1967

$$T_{orig} = T_{seq} + T_{par}$$

$$s = \frac{T_{seq}}{T_{orig}}, f = \frac{T_{par}}{T_{orig}}, p \text{ is speedup of } T_{par}$$

$$T_{new} = T_{seq} + \frac{T_{par}}{p} = T_{orig} - T_{par} + \frac{T_{par}}{p}$$

$$\text{Overall speedup} = \frac{T_{orig}}{T_{new}} = \frac{T_{orig}}{T_{orig} - T_{par} + \frac{T_{par}}{p}} = \frac{1}{(1-f) + \frac{f}{p}} = \frac{1}{\boxed{s} + \frac{f}{p}}$$

There may be more!
Bottleneck!



Amdahl's Law Class Exercise



How to Fix a Bottleneck?

First find it!

Change the algorithm

The previous bottleneck no longer applies—e.g., concurrency

Find a fast path

Make the bottleneck rare—normal case is fast, and some progress is made for the worst case

Slow path time, T_s and Fast path time, T_f

Slow path probability, $p \ll 1$

Mean time $\langle T \rangle \approx pT_s + T_f$

How slow is this over the fast path (the ceiling)?

$$\frac{(pT_s + T_f)}{T_f} = 1 + p \left(\frac{T_s}{T_f} \right)$$

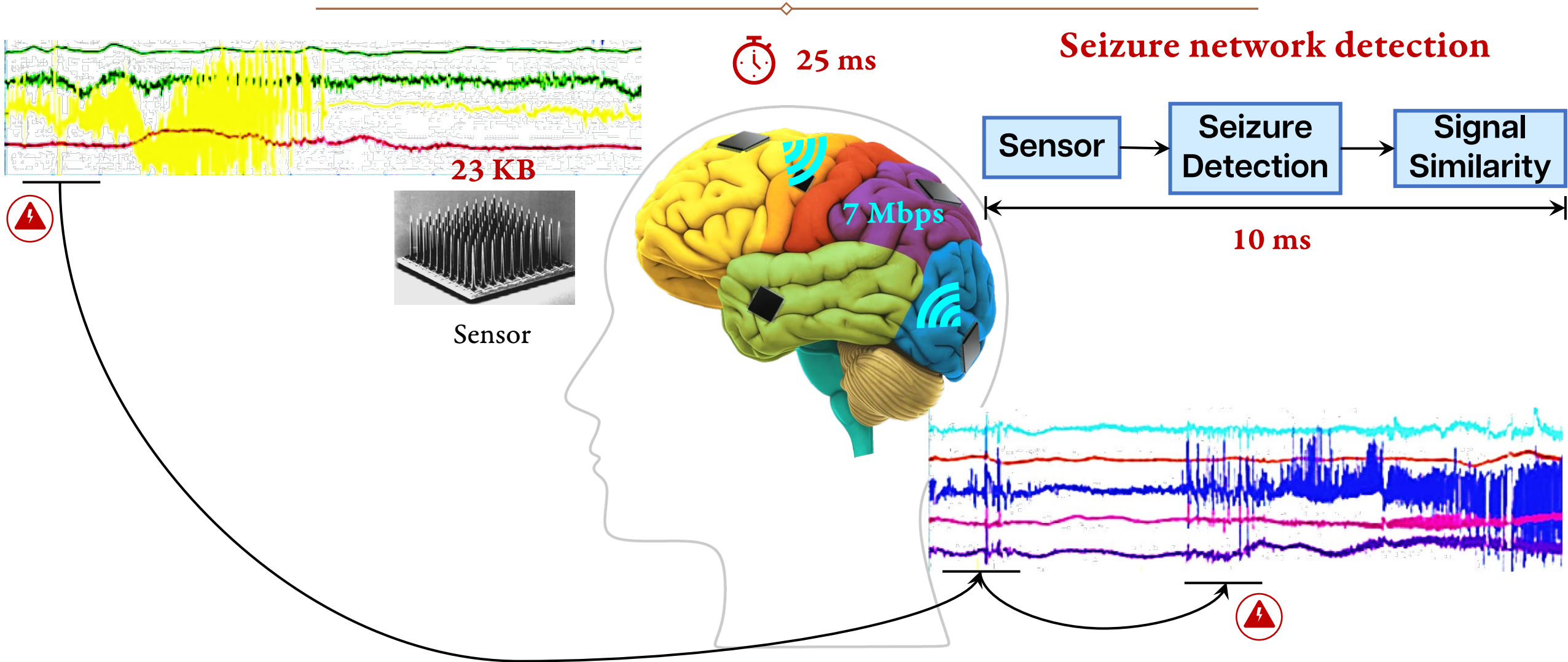
How fast is this over the slow path (the floor)?

$$\frac{T_s}{pT_s + T_f} = \frac{1}{p + \frac{T_f}{T_s}}$$

What can we say about the maximum speedup based on Amdahl's law?



Example from a BCI Processor (SCALO)



Rewriting Applications to Filter Communication

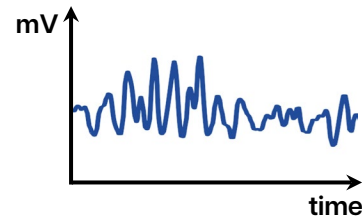
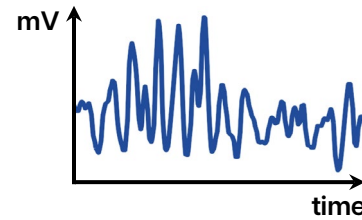
Locality sensitive hashing

Euclidean Distance: $O(N)$

Cross correlation: $O(kN)$

Dynamic Time Warping: $O(N^2)$

Earth mover's distance: $O(N^3 \log N)$



00110010

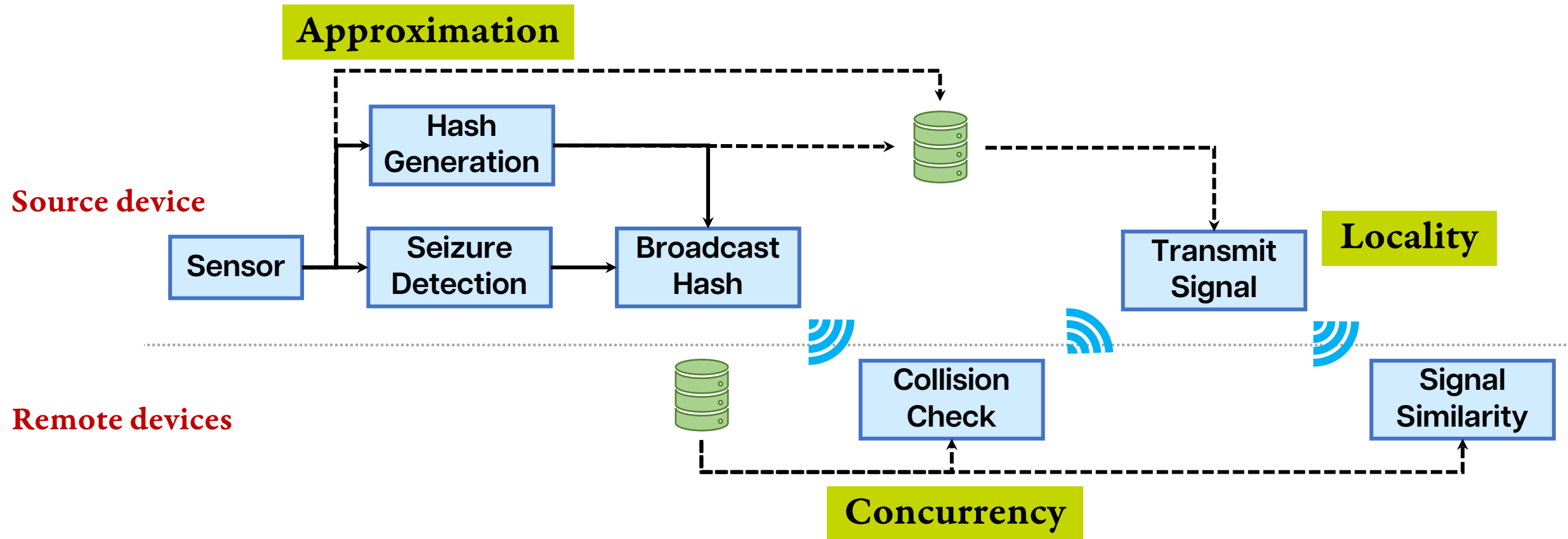
Equality check!

240 B

1 B

Rewriting Applications to Filter Communication

Created a fast path!



More ways to Improve Efficiency

Exploit technology

e.g., at 12 nm, area not a key constraint for BCIs.
NVMs are a feasibility

Approximate

Filter, compress, sample,
precision, stale data

Predict

Relax synchronization, “correctness”
(expectations of correctness)—e.g.,
HogWild! NeurIPS 2011—but,
know how correct you are!

Locality

Keep data small, keep close

Regroup

Batch, when one-time costs are high and non-recurring—e.g., cache data block access

Fragment, when it enables concurrency—
e.g., **pipelining**,
streaming, sharding.

Independent
components

Centralized vs
distributed



Takeaways

2-page project proposals due 9/2
Signal processing lab due 9/16

What is computer architecture?

Historically, the ISA; but now encompasses organization

What are the goals?

Mnemonic: Simple Timely Efficient Adaptable Dependable Yummy

How to estimate impact of fixing bottlenecks?

Amdahl's law

How to fix bottlenecks?

Algorithms, adding a fast path

How to improve efficiency?

Technology, approximation, locality, regroup



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- Hand with spoon: public domain freepng
- Signals: <https://www.nature.com/articles/nrn3724>
- Thought clouds: F. Willett et al./*Nature* 2021/Erika Woodrum, <https://med.stanford.edu/neurosurgery/news/2022/bci-award>. <https://www.the-scientist.com/news-opinion/brain-computer-interface-user-types-90-characters-per-minute-with-mind-68762>
- Picture of scientists: <https://www.cs.auckland.ac.nz/~brian/rutherford8.html> (original: Pierre de Latil), Bush (Carnegie Science), Others (Wikipedia)
- Flowchart: Pause08 – flaticon.com
- Digital brain: Smashicons – flaticon.com
- Server rack: upklyak – freepik.com
- Quantum processor icons created by Paul J. - Flaticon
- Arm, Lotus: Adobe stock
- Quantum processor: Rigetti computing
- Images of implanted users: Top: Case Western Reserve University (<https://thedaily.case.edu/man-quadruplegia-employs-injury-bridging-technologies-move-just-thinking/>), Bottom: Jan Scheuermann (University of Pittsburgh/UPMC; <https://www.upmc.com/media/news/bci-press-release-chocolate>)
- Images of wearable BCIs: Cognixion, NextMind
- Types of BCIs: “Brain–computer interfaces for communication and rehabilitation,
- Illustrative BCI: Neuralink
- Electrodes: “Electrochemical and electrophysiological considerations for clinical high channel count neural interfaces”, Vatsyayan et al.
- Form factors: Neuropace, Medtronic, Bloomberg, “Fully Implanted Brain–Computer Interface in a Locked-In Patient with ALS” by Vansteensel et al., Blackrock Neurotech
- Jose Delgado’s video: Online, various sources (CNN, Youtube)
- Video of Kennedy and Ramsey: Online, various sources (Youtube, Neural signals)

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