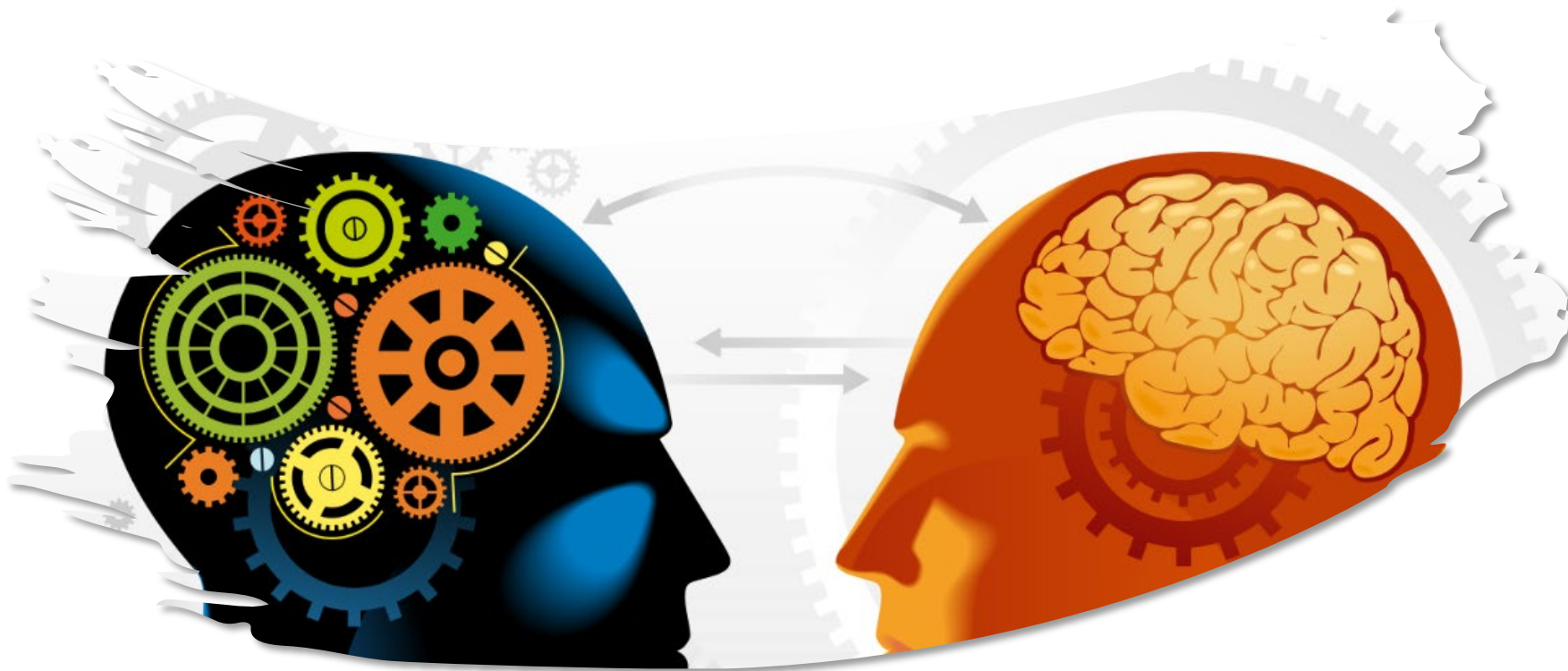




Building the Infinite Brain

COMP 690 (193)

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Quick Review

2-page project proposals due 9/2
Signal processing lab due 9/16

What is computer architecture?

Historically, the ISA; but now encompasses organization

What are the goals?

Mnemonic: Simple Timely Efficient Adaptable Dependable Yummy

How to estimate impact of fixing bottlenecks?

Amdahl's law

How to fix bottlenecks?

Algorithms, adding a fast path

How to improve efficiency?

Technology, approximation, locality, regroup



For Today

- Quick review
- **Pipelining**

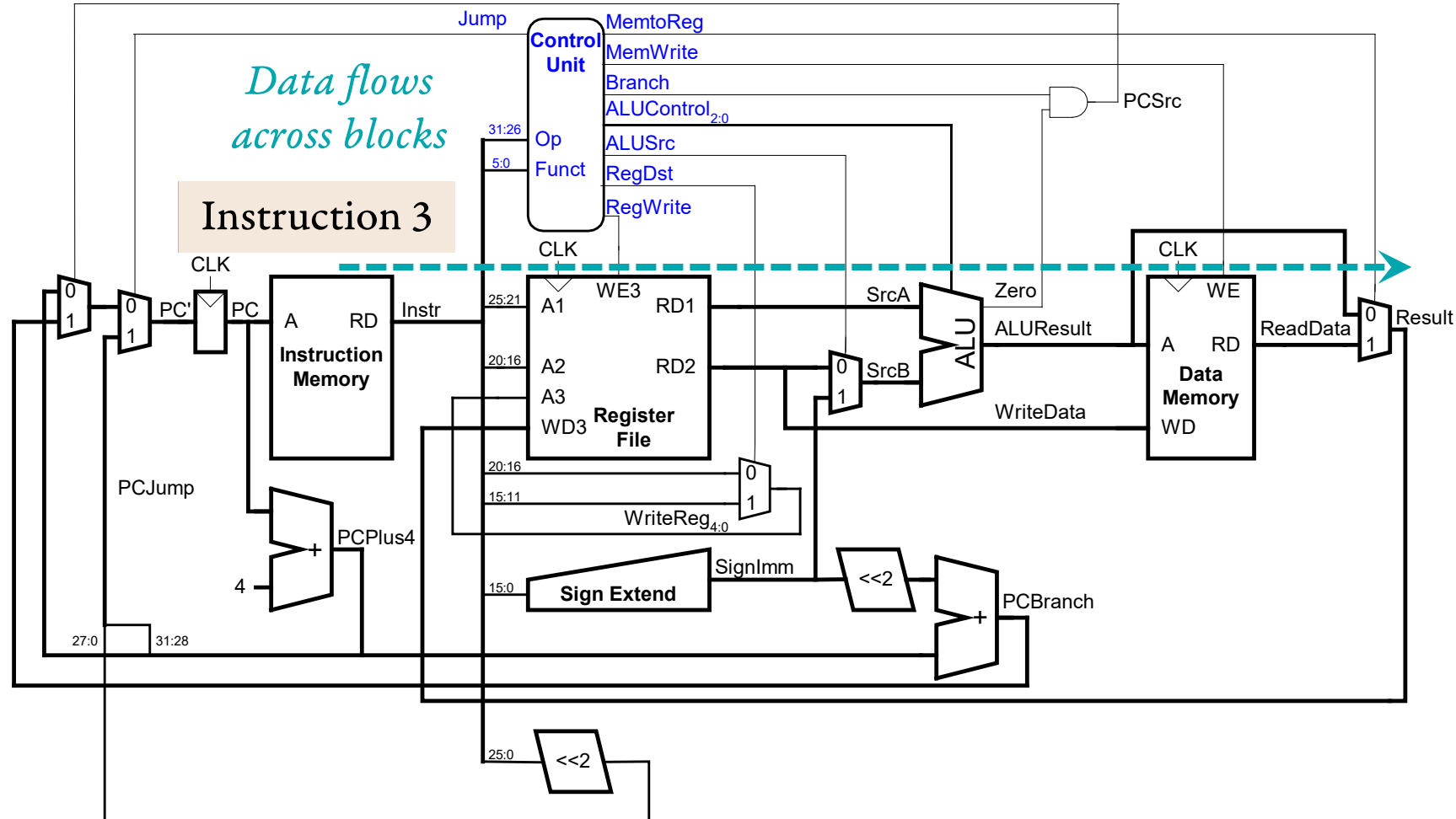


Motivation

Is all the hardware fully being used all the time, i.e., is there resource efficiency?

Latency: τ

Throughput: $\frac{1}{\tau}$



Fetch → Decode → Execute → Memory → Write-back

Regroup: Pipelining

$$\tau_{\text{pipeline}} \neq \tau_{\text{original}}$$

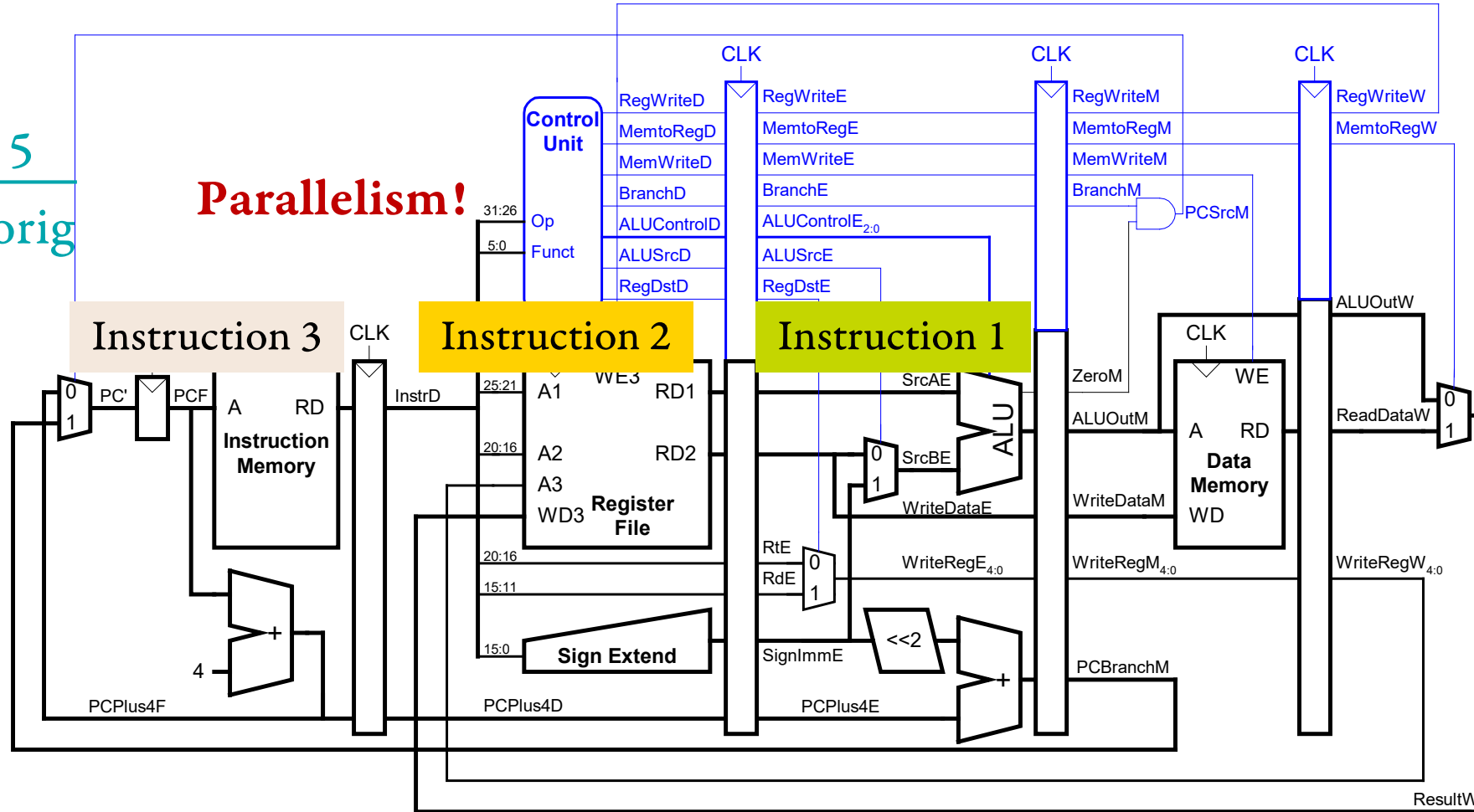


Divide the resource into stages

Latency: τ_{orig}

Throughput: $\frac{5}{\tau_{\text{orig}}}$

Parallelism!



Fetch (IF)

Decode (ID)

Execute (EX) Memory (MEM) Write-back (WB)



Pipelining: Assessing Goals

Improve throughput, utilization

Sacrifice latency, simplicity, power



Pipeline Performance

$$\sum \tau_i = \tau$$

$$\text{Latency: } n \times \max(\tau_i) \geq \tau$$

$$\text{Throughput: } \frac{1}{\max(\tau_i)} \leq \frac{n}{\tau}$$

“Optimal Pipelining in Supercomputers”, Kunkel and Smith, ISCA’86

“The Optimal Logic Depth Per Pipeline Stage is 6 to 8 FO4 Inverter Delays”, Hrishikesh et al., ISCA’02



Exercise

$\tau_i: 8, 12, 10$ $\Delta_{\text{register}}: 2$

Latency, throughput, speedup?

$$\text{Execution time} = \frac{\text{instructions}}{\text{program}} \times \frac{\text{cycles}}{\text{instruction}} \times \frac{\text{time}}{\text{cycle}}$$



Pipeline Hazards

Structural

Multiple instructions need to use the same resource (execution unit, memory port etc.)

Data

Subsequent instructions need to wait for a prior instruction to complete

ADD R1, R2, R3
ADD R4, R5, R1

Control

Subsequent instructions need to be determined by a prior instruction

→BEQ R1, label
ADD R7, R6, R7

$$CPI_{\text{pipeline}} = CPI_{\text{ideal}} (=1) + \text{Stall CPI}$$

$$\text{Pipeline speedup} = \frac{\text{Time}_{\text{original}}}{\text{Time}_{\text{pipeline}}} = \frac{CPI_{\text{original}} \times \text{Period}_{\text{original}}}{CPI_{\text{pipeline}} \times \text{Period}_{\text{pipeline}}} = \frac{\text{Pipeline depth}}{1 + \text{Stall CPI}}$$



Exercise: Examining Throughput With Stalls

Total gate delay per instruction: **D**

Overhead per stage: **Δ**

Average stalls per instruction per stage: **S**

Number of stages : **n**

$$\text{CPI}_{\text{pipeline}} = 1 + S \times n$$

$$\text{Period} = \frac{D}{n} + \Delta$$

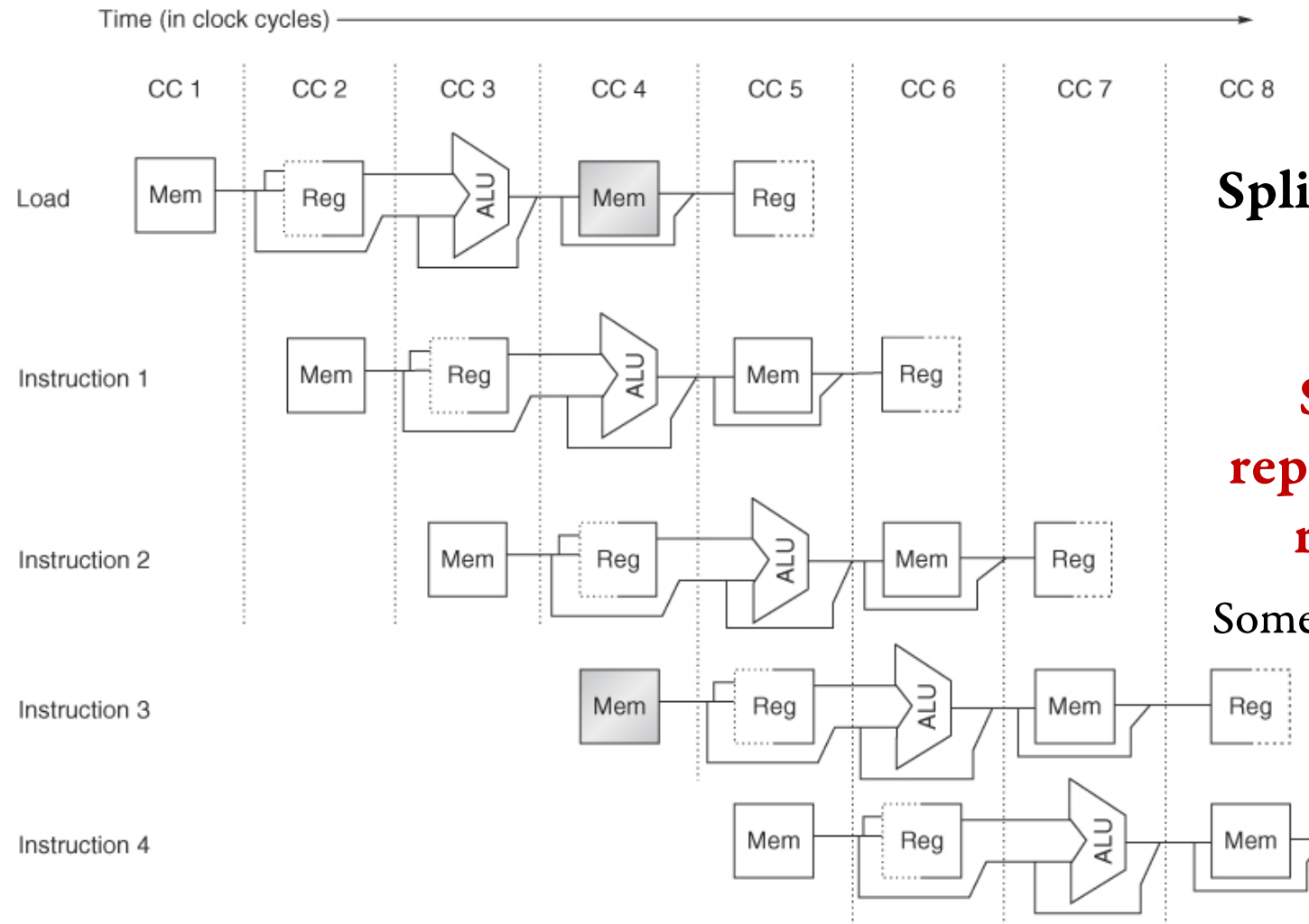
$$\text{Throughput: } \frac{\text{Instructions}}{\text{second}} = \text{IPC} \times \text{Frequency}$$

For some choices of D (about 100), Δ (about 1), S (about 0.05–0.2), plot throughput vs n



Pipeline Hazards: Structural

Recall: “Independent” “Divide and conquer”



Split I and D caches!

**Split, pipeline,
replicate, streamline
resource access**

Some instructions may take
multiple cycles

Pipeline Hazards: Data

Read after a Write (RAW) – data dependence

ADD R1 $\leftarrow$ R1, 1

ADD R2 $\leftarrow$ R1, R3

Write after a Write (WAW) – output dependence

Write after a Read (WAR) – anti dependence

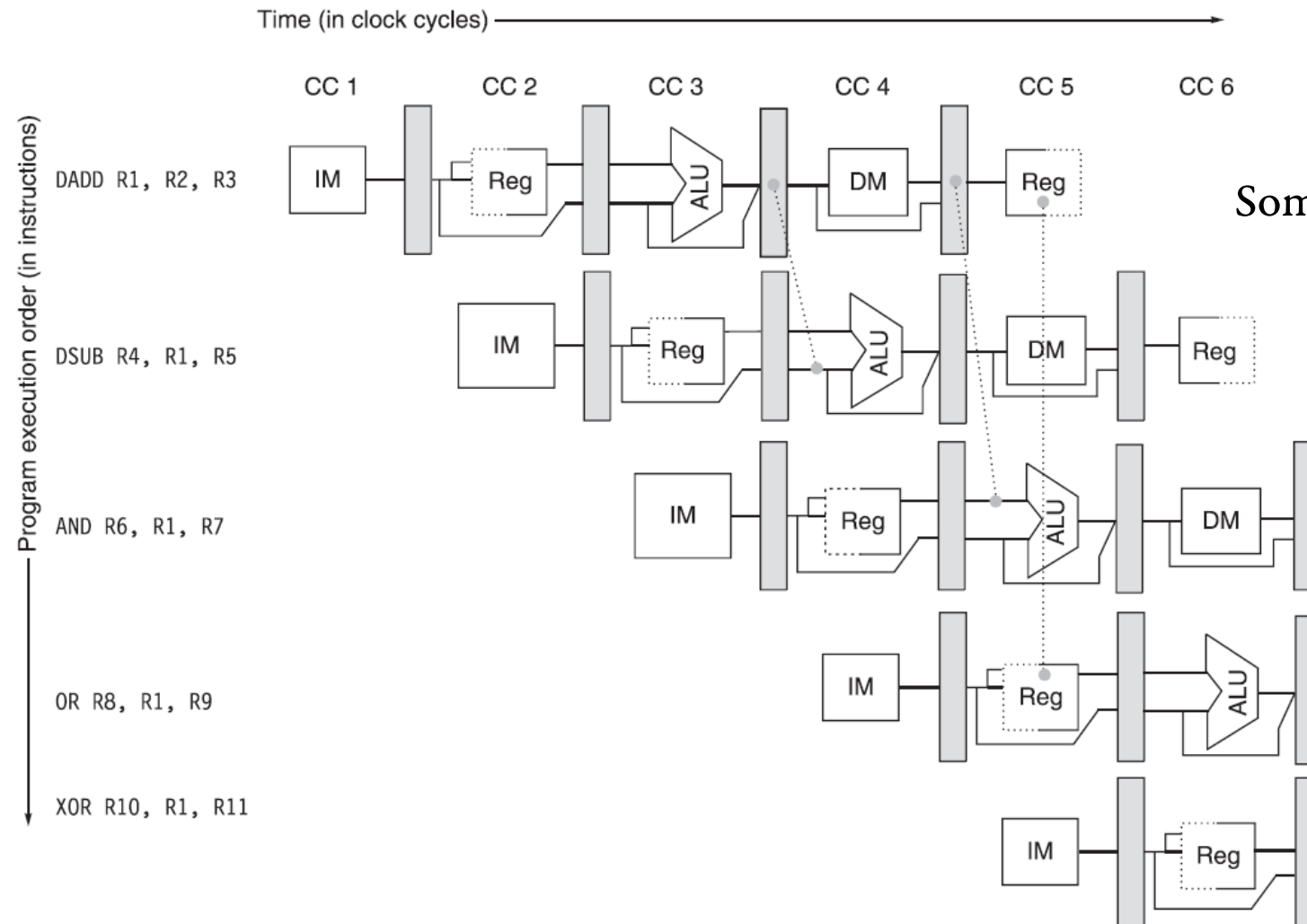
When do these matter?



Data Hazard Example

How to solve?

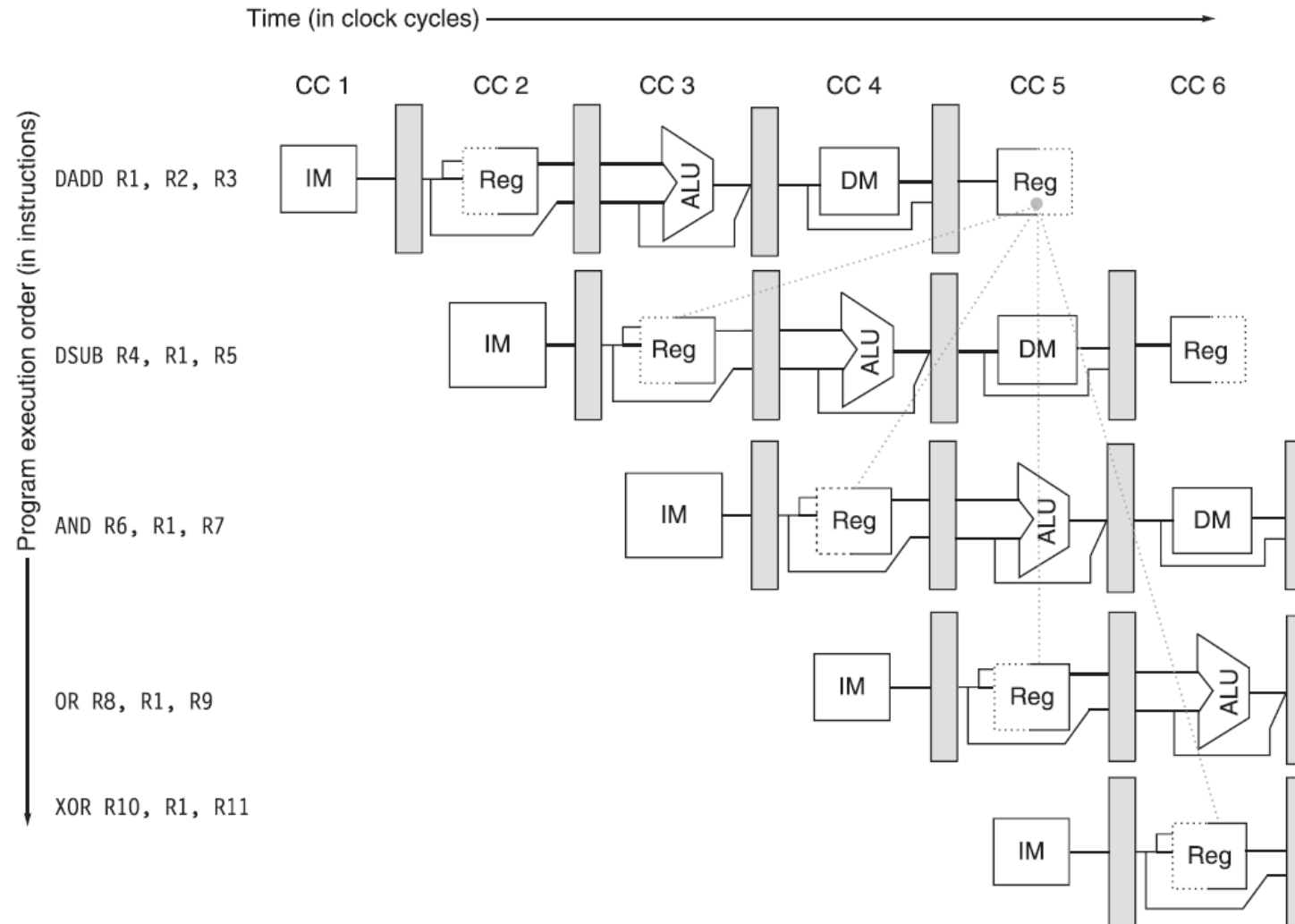
“Eager”: Bypassing/forwarding/“short circuiting”



Some instructions may take multiple cycles

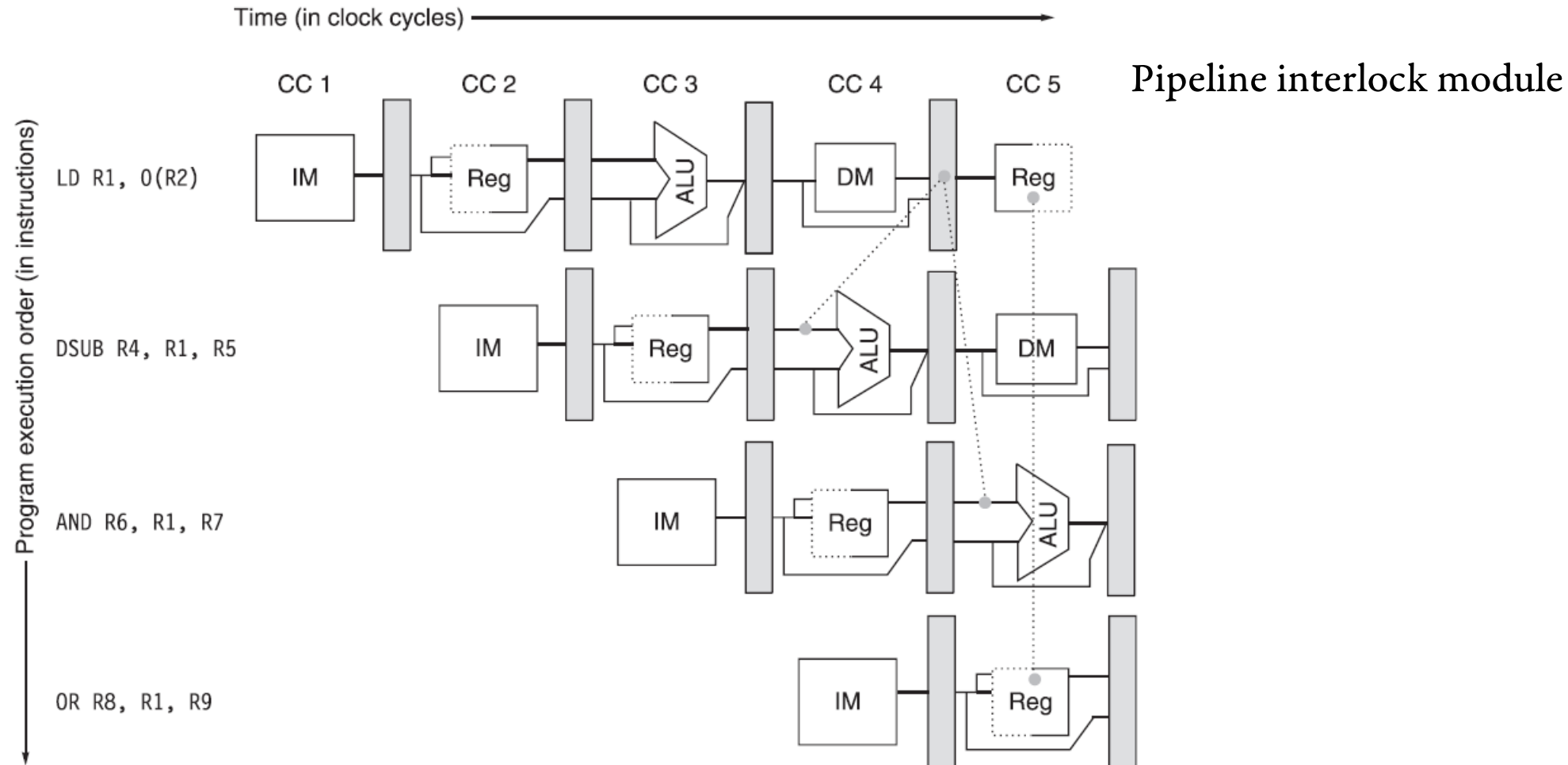
Data Hazard Example

How to solve?



What About This Example?

Unavoidable stall!



Another solution when feasible: compiler reordering

Pipeline Hazards: Control

Branch instruction	IF	ID	EX	MEM	WB		
Branch successor		IF	IF	ID	EX	MEM	WB
Branch successor + 1				IF	ID	EX	MEM
Branch successor + 2					IF	ID	EX

Branch stall costs: Branch frequency $\times$ Branch penalty

How to solve?

“Eager”: Delay slot (make use of the next instruction that gets fetched)

“Speculate”: Branch prediction (check if PC is PC+1 or the branch target)

2-bit predictors, tournament predictors, machine learning etc.

<https://ericrotenberg.wordpress.ncsu.edu/cbp2025-workshop-program/>



Takeaways

What is pipelining?

Splitting work into many components executed independently, and passed in a chain

Why pipelining?

Increases efficiency via parallelism

*Pipelining was conceived to meet hard design goals—
IBM Stretch, ILLIAC etc.
BCI processing creates a similar need!*

What are the challenges in pipelining?

Hazards: structural, data, control

How to fix hazards?

Concurrency (structural), eager (forwarding data), eager or speculative (branch delays, prediction)

What systems design principles does pipelining touch?

Tradeoff simplicity for efficiency, leveraging parallelism through regrouping



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- Electrodes: “Electrochemical and electrophysiological considerations for clinical high channel count neural interfaces”, Vatsyayan et al.
- Form factors: Neuropace, Medtronic, Bloomberg, “Fully Implanted Brain–Computer Interface in a Locked-In Patient with ALS” by Vansteensel et al., Blackrock Neurotech
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