Raghavendra Pradyumna Pothukuchi

Yale University

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Research Interests

Primary area: Computer architecture and systems

Secondary areas: Brain-computer interfacing, Quantum computing, Brain-inspired AI hardware, Cognitive modeling, Formal control, Energy and power efficiency, Security, Machine learning, Datacenters and cloud, Compilers

Current Focus: **Building the Infinite Brain: Machines that Talk to the Brain and Think Like the Mind**

PhD Dissertation: **Intelligent Systems for Efficiency and Security**

Academic Appointment

Yale University **2021–Current**
Associate Research Scientist, NSF Computing Innovation Fellow (CIFellow)
Mentors: Abhishek Bhattacharjee (Yale) and Jonathan Cohen (Princeton)

Education

Yale University **2020–2021**
Postdoctoral Associate
Mentors: Abhishek Bhattacharjee (Yale) and Jonathan Cohen (Princeton)

University of Illinois at Urbana-Champaign (UIUC) **2020**
Ph.D. in Computer Science (CS)
Advisor: Josep Torrellas

University of Illinois at Urbana-Champaign **2014**
M.S. in Computer Science 3.96/4.00

Birla Institute of Technology & Science, Pilani, India **2011**
B.E. (Hons.) Electrical and Electronics Engineering (EEE) 10.00/10.00

Honors and Awards

- **Blavatnik Regional Award for Young Scientists, The New York Academy of Sciences,** *laureate in Physical Sciences & Engineering across New York, New Jersey, and Connecticut,* 2024
- **IEEE Micro Top Picks in Computer Architecture,** *research selected as one of the 12 top published papers in all of computer architecture,* 2024
- **Best Paper Award,** *International Symposium on Computer Architecture (ISCA),* 2023
- **Spotlight Research,** *Wu Tsai Institute, Yale University,* 2023
- **Young Researcher, Heidelberg Laureate Forum (HLF),** *selected as one of the 100 young researchers in computer science worldwide invited to attend HLF,* 2022.
- **IEEE Micro Top Picks in Computer Architecture,** *research selected as one of the 12 top published papers in all of computer architecture,* 2021
- **CRA NSF Computing Innovation Fellow (CI Fellow)**, *one of the 69 researchers across USA awarded by the Computing Research Association (CRA) and National Science Foundation (NSF),* 2021-2024
  Press release: https://cccblog.org/2021/07/22/announcing-the-2021-computing-innovation-fellows/

- **Swati and Mukul Chawla Scholarship,** *Parallaxes Capital, UIUC,* 2020
- **Featured Cover Article ,** *IEEE Control Systems,* 2020
- **IEEE Computer Society Lance Stafford Larson Paper Award,** *2nd prize* (2019) *and 3rd prize* (2018)
- **W. J. Poppelbaum Award** *for architecture design creativity, Dept. of CS, UIUC,* 2018
- **Rising Stars in Computer Architecture***, Georgia Institute of Technology,* 2018
- **Mavis Future Faculty Fellow,** *College of Engineering, UIUC,* 2017
- **ACM Student Research Competition winner,** *International conference on Parallel Architectures and Compilation Techniques (PACT),* 2017
- **Certificate in Foundations of Teaching,** *Center for Innovation in Teaching and Learning, UIUC,* 2017
- **Best Paper Award nominee,** *PACT,* 2017
- **Best Graduating Student,** *Prof. L. K. Maheshwari foundation, BITS Pilani,* 2011
- **University Gold Medal** *for outstanding academic achievement, BITS Pilani,* 2011
- **GE Innovation Award,** *John F. Welch Technology Centre, General Electric (GE),* 2010
- **University Merit Scholarship,** *BITS Pilani,* 2007 – 2011

Publications

Conferences

- **The QUATRO Application Suite: Quantum Computing for Models of Human Cognition**
  R. P. Pothukuchi, L. Lufkin, Y Shen, A. Simon, R. Thorstenson, B. E. Trevisan, M. Tu, M. Yang, B. Foxman, V. S. Pothukuchi, G. Epping, T. H. Kyaw, B. J. Jongkees, Y. Ding, J. Busemeyer, J. D. Cohen, A. Bhattacharjee
  Submitted (*available on arXiv)*, 2023.
- **PowerGrad: ML-based Hierarchical Power Management of Power-Limited Serverless Systems**
  H. Nam, R. P. Pothukuchi, A. Buyuktusunoglu, A. Amarnath, P. Bose, J. Torrellas
  Submitted, 2023.
- **Defensive AML: Adversarial Machine Learning as a Practical Architecture Defense for Side Channels**
  H. Nam, R. P. Pothukuchi, B. Li, N. S. Kim, J. Torrellas
  International conference on Parallel Architectures and Compilation Techniques (**PACT**), Sep 2024.
- **Mitigating Catastrophic Forgetting in Long Short-Term Memory Networks**
  K. Joshi, R. P. Pothukuchi, A. Wibisano, A. Bhattacharjee
  arXiv, 2023.
- **SCALO: An Accelerator-Rich Distributed System for Scalable Brain-Computer Interfacing**
  K. Sriram*, R. P. Pothukuchi*†, O. Ye, M. Gerasimiuk, M. Ugur, R. Manohar, A. Khandelwal, A. Bhattacharjee
  *Joint first authors †Lead PI
  International Symposium on Computer Architecture (**ISCA**), Jun 2023. [21% acceptance]
  Best Paper Award
  IEEE Micro Top Picks in Computer Architecture
- **Distill: Domain-Specific Compilation for Cognitive Models**
  J. Veselý*, R. P. Pothukuchi*, K. Joshi, S. Gupta, J. D. Cohen, A. Bhattacharjee
  *Joint first authors
  International Symposium on Code Generation and Optimization (**CGO**), Apr 2022. [29% acceptance]

» **Maya: Using Formal Control to Obfuscate Power Side Channels**
R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, A. Schwing, J. Torrellas
International Symposium on Computer Architecture (**ISCA**), Jun 2021. [19% acceptance]
IEEE Micro Top Picks in Computer Architecture

» **Tangram: Integrated Control of Heterogeneous Computers**
R. P. Pothukuchi, J. Greathouse, K. Rao, L. Piga, C. Erb, P. Voulgaris, J. Torrellas
International Symposium on Microarchitecture (**MICRO**), Oct 2019. [23% acceptance]
2nd Prize, IEEE Computer Society Lance Stafford Larson Paper Award

» **Structured Singular Value Control for Modular Resource Management in Multilayer Computers**
R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, J. Torrellas
IEEE Conference on Decision and Control (**CDC**), Dec 2018. [60% acceptance]

» **Yukta: Multilayer Resource Controllers to Maximize Efficiency**
R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, J. Torrellas
International Symposium on Computer Architecture (**ISCA**), Jun 2018. [17% acceptance]

» **Sthira: Systematically Controlling the Error Rates in Variation-Prone Networks-on-Chip for Energy Efficiency**
R. P. Pothukuchi, A. Ansari, B. Gopireddy, J. Torrellas
International conference on Parallel Architectures and Compilation Techniques (**PACT**), Sep 2017. [23% acceptance]
Best Paper Nominee

» **Using Multiple Input, Multiple Output Formal Control to Maximize Resource Efficiency in Architectures**
R. P. Pothukuchi, A. Ansari, P. Voulgaris and J. Torrellas
International Symposium on Computer Architecture (**ISCA**), Jun 2016. [20% acceptance]
3rd Prize, IEEE Computer Society Lance Stafford Larson Paper Award

Workshops (peer-reviewed)

» **The Interplay of Computing, Ethics, and Policy in Brain-Computer Interface Design**
M. Ugur, R. P. Pothukuchi, A. Bhattacharjee
Workshop on Hot Topics in Ethical Computer Systems (**HotEthics**), May 2024.

» **Towards Forever Access for Implanted Brain-Computer Interfaces**
M. Wu, R. P. Pothukuchi, A. Bhattacharjee
Workshop on Hot Topics in Ethical Computer Systems (**HotEthics**), May 2024.

» **Swapping-Centric Neural Recording Systems**
M. Wu, R. P. Pothukuchi, A. Bhattacharjee
Non-Volatile Memories Workshop (**NVMW**), Mar 2024.

» **Prefetching Using Principles of Hippocampal-Neocortical Interaction**
M. Wu, K. Joshi, A. Sheinberg, G. Cox, A. Khandelwal, R. P. Pothukuchi, A. Bhattacharjee
Workshop on Hot Topics in Operating Systems (**HotOS**), Jun 2023. [26% acceptance]
Yale Wu Tsai Institute "Spotlight Research"

Journals

» **Distributed Brain-Computer Interfacing with a Networked Multi-Accelerator Architecture**
R. P. Pothukuchi*, K. Sriram*, O. Ye, M. Gerasimiuk, M. Ugur, R. Manohar, A. Khandelwal, A. Bhattacharjee
*Joint first authors
IEEE Micro, Top Picks Special Edition, to appear. [10% acceptance, Impact factor 3.6]

» **HALO: Hardware-Software Co-Designed Processor for Brain-Computer Interfaces**
I. Karageorgos, K. Sriram, X. Wen, J. Vesely, N. Lindsay, M. Wu, L. Khazan, R. P. Pothukuchi, R. Manohar, A. Bhattacharjee
IEEE Micro, Hot Chips Special Edition, May 2023.

» **Maya: Using Formal Control to Obfuscate Power Side Channels**
R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, A. Schwing, J. Torrellas
IEEE Micro, Top Picks Special Edition, Jul-Aug 2022. [11% acceptance, Impact factor 2.821]

» **Control Systems for Computer Systems: Making Computers Efficient with Modular, Coordinated and Robust Control**
R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, J. Torrellas
IEEE Control Systems (**CSM**), Mar 2020. [Impact factor 11.119]
Cover Highlight Article

Patents

» **A Distributed System of Computer Architectures**
A distributed system of ultra-low-power accelerator rich computer architectures with two-step hash-based communication, realized for a multi-region brain-computer interface
K. Sriram, R. P. Pothukuchi, R. Manohar, A. Khandelwal, A. Bhattacharjee
U.S. Provisional Patent Application No. 63/508,760, 2023.

» **Distributed Multi-Input Multi-Output Control Theoretic Method to Manage Heterogeneous Systems**
A distributed resource control system for efficient heterogeneous or distributed computers
R. P. Pothukuchi, J. Greathouse, L. Piga
US Patent 10,928,789, 2021.

Tech Reports

» **Designing a Robust Controller for Obfuscating a Computer's Power**
R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, J. Torrellas
[Online] http://iacoma.cs.uiuc.edu/iacoma-papers/isca21_1_tr.pdf, Jun 2021.

» **A Guide to Design MIMO Controllers for Architectures**
R. P. Pothukuchi, J. Torrellas
[Online] http://iacoma.cs.uiuc.edu/iacoma-papers/mimoTR.pdf, Apr 2016.

Posters and Poster Papers

» **Quantum, Cognition and Computer Systems**
Lead PI and presenter: R. P. Pothukuchi
Co-PIs (alphabetical order): A. Bhattacharjee, J. Busemeyer, J. D. Cohen, Y. Ding, B. Jongkees, and T. H. Kyaw
Students (alphabetical order): Y. Abukhadra, N. Ahn, Y. D. Chua, G. Epping, B. Foxman, C. Hann, L. Rosendahl, Y. J. Shen, A. Simon, B. Trevisan, M. Tu, J. Wang, M. Yang
Heidelberg Laureate Forum, Sep 2022.

» **Multilayer Compute Resource Management with Robust Control Theory**
R. P. Pothukuchi, S. Y. Pothukuchi, P. Voulgaris, J. Torrellas
International Conference on Parallel Architectures and Compilation Techniques (**PACT**), Sep 2017.
Winner, ACM Student Research Competition

» **Remote Experimentation of "No-load Tests on a Transformer" in Electrical Engineering**
Pradyumna, P. R., Tarun, C.K.S., Bhanot, S
International Conference on Engineering Education: Innovative Practices and Future Trends (**AICERA**), Jul 2012.

Grants

PI/Co-PI

» **"Next-Generation Computer Architecture for Emergent Symbolic Binding Networks"**, *under preparation,*
PI: Abhishek Bhattacharjee, Co-PI: Jonathan D Cohen, John Lafferty, Raghavendra Pradyumna Pothukuchi.

» **"A Flexible Ultra-Low-Power Processors for Implantable Brain-Computer Interfaces"**, *submitted, NSF MRI*
PI: Abhishek Bhattacharjee, Co-PI: Rajit Manohar, Hitten Zaveri, Raghavendra Pradyumna Pothukuchi.

Writing Experience

» **"CSR: Medium: Effective Control to Maximize Resource Efficiency in Large Clusters; Hardware, Runtime, and Compiler Perspectives"**, *NSF Award #1763658,* 2018
PIs: Josep Torrellas, Laxmikant Kale, David Padua at UIUC.
Media coverage: https://dailyillini.com/news/2018/11/01/ui-professors-receive-1-2-million-grant-to-improve-computer-efficiency/

» **"SPX: Secure, Highly-Parallel Training of Deep Neural Networks in the Cloud Using General-Purpose Shared-Memory Platforms"**, *NSF Award #1725734,* 2017.
PIs: Josep Torrellas, Christopher Fletcher at UIUC.

Industry Experience

AMD Research, Austin, USA **Mar'18–May'18, May'17–Dec'17**
Coop Intern

» Developed a modular composable resource control network for heterogeneous computers

» Prototyped the proposed design on a 2 CPU-GPU node

» Filed for a patent and authored a paper that was accepted at MICRO 2019

Nvidia Graphics, Bangalore, India **Aug'11–Jun'12**
ASIC Design Engineer

» Closed timing in multiple chips at 28 nm technology

» Analyzed USB 2.0 IO modules in Tegra 4 mobile SoC, high-speed memory interface paths in Tesla GPGPU for high performance computing and Kepler GPU for desktop graphics

Nvidia Graphics, Bangalore, India **Spring'11**
Hardware Design Intern

» Developed a SPICE based timing analysis framework of multi-voltage IO paths in Nvidia's first 28 nm GPU

Indira Gandhi Center for Atomic Research, Kalpakkam, India **Summer'09**
Research Intern

» Developed a micrometer positioner read-out using a Programmable System on Chip (PSoC) based embedded system, and LabVIEW virtual instrumentation

Tutorials & Demos

R. P. Pothukuchi, **"Brain-Computer Interfaces"**, *held at the International Symposium on Microarchitecture* (**MICRO**), 2023. Demo and poster.

R. P. Pothukuchi, H. Hoffmann, K. Rao, J. Torrellas, **"Combining Machine Learning and Control Theory for Computer Architecture (MCAt)"**, *held at the International Symposium on Microarchitecture* (**MICRO**), 2019. http://iacoma.cs.uiuc.edu/mcat/index.html [55 participants]

Invitations to Workshops

"5 Year Update to the Next Steps in Quantum Computing Workshop", *Computing Community Consortium* , 2023. https://cra.org/ccc/events/5-year-update-to-the-next-steps-in-quantum-computing-workshop/

"Planning Workshop on Quantum Computing", held at *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2023.

Invited Talks

Building the Infinite Brain

- New York University, April 2024
- University of Southern California, April 2024
- University of Virginia, Charlottesville, April 2024
- University of Michigan, Ann Arbor, March 2024
- Carnegie Mellon University, March 2024
- The NSF AI Institute for Edge Computing (Athena), March 2024
- University of North Carolina at Chapel Hill, February 2024

Quantum Systems for Cognitive Modeling

- Yale Quantum Institute, October 2023

Machines that Talk to the Brain and Think Like the Mind

- University of Pennsylvania, October 2023
- New York University, October 2023
- Rutgers University, October 2023

Hull: A New Distributed and Scalable Brain-Computer Interfacing Architecture

- Neurostimulation Research Meeting, Yale University, November 2023

Intelligent Systems for Extreme-Efficiency and Security

- Georgia Institute of Technology, February 2021
- University of California at Los Angeles, February 2020
- Pennsylvania State University, February 2020
- Yale University, November 2019

Maya: Using Formal Control to Obfuscate Power Side-channels

- Intel Side Channel Academic Program, Workshop, Intel, May 2021
- Security and Privacy Research at Illinois (SPRAI), UIUC, September 2019

Extreme-Efficiency Computing

- Indian Institute of Sciences (IISc), Bengaluru, India, January 2019
- Intel Research, Bengaluru, India, January 2019
- Indian Institute of Technology (IIT), Delhi, India, January 2019
- Rising Stars in Computer Architecture Workshop, Georgia Tech, September 2018

Mentoring

Research Mentor **Sep'20–Curr.**

Yale University

» Mentored 4 PhD students: two on Brain-Computer Interfaces (present, M. Ugur; past, K. Sriram), one on brain-inspired memory system design (M. Wu), and one on LSTM continual learning (K. Joshi).

» Mentored 15 undergraduates on using quantum computing for cognitive modeling

» My students received an **NSF Graduate Research Fellowship**, and several undergraduate fellowships at Yale like the **STARS II program**, **Wu Tsai summer research fellowship**, **Andy Keidel summer grant**, and the **Branford Richter Fellowship**, and have been admitted to top graduate programs at MIT, Princeton, UC Berkley, and Yale.

Mavis Mentor **Aug'16–Aug'17**

College of Engineering, UIUC

» Mentored 2 masters students towards their thesis.

MUSE Mentor **Aug'16–Aug'17**

College of Engineering, UIUC

MUSE: Mentoring Undergraduate Students in Engineering

» Mentored a sophomore in an introductory machine learning research project

Teaching

Computer Architecture **Fall'16**

Teaching substitute, Yale

CPSC 420: Foundational computer architecture course (30 students)

» Taught four lecture sessions on cache coherency and memory consistency

Parallel Computer Architecture **Spring'17**

Teaching Assistant, UIUC

CS 533: Graduate course on advanced architecture topics (19 students)

» Taught three lectures, created and graded homeworks, organized office hours

Energy Efficient Computer Architecture **Fall'16**

Teaching Assistant, UIUC

CS 598: Discussion course on recent ideas for energy efficient architectures (10 students)

» Moderated and provided insights on discussions during four lecture sessions

Computer System Organization **Fall'15**

Teaching Assistant, UIUC

CS 433: Early graduate/senior course on computer architecture (25 students)

» Taught two lectures, designed homeworks and examinations, and organized office hours

Microelectronic Circuits **Fall'10**

Teaching Assistant, BITS Pilani

Course on the analysis and design of analog MOS circuits (~80 students)

» Led micro-teaching classes, and laboratory sessions on Cadence Virtuoso and Eldospice tools

Engineering Graphics **Fall'08**

Teaching Assistant, BITS Pilani

Course on introductory computer aided drawing (~120 students)

» Developed AutoCAD laboratory modules and organized lab hours

Service

Organizational Service

Computer Architecture Student Association (CASA) **2020–Curr.**
Co-founder
https://www.comparchsa.org/

» CASA's vision is to promote student wellbeing and a sense of belonging in the computer architecture community

» Worked with SIGARCH and TCCA to establish CASA

» Original proposal: http://ieeetcca.org/wp-content/uploads/2020/05/Arch_student_wellbeing_27MAY.pdf

Students Advising on Graduate Education (SAGE) Board **Aug'17–Aug'18**
Graduate College, UIUC

» Advisory member to the Dean on matters related to graduate affairs

Engineering Graduate Student Advisory Committee (EGSAC) **Aug'16–Aug'17**
College of Engineering, UIUC

» Advisory member to the Dean, College of Engineering

» Proposed an interdisciplinary fellowship, events to promote interdisciplinary research, and student wellness

Computer Science Graduate Academic Council (CSGAC) **Aug'15–Aug'17**
Dept. of CS, UIUC

» Advisory member to the department on improving graduate academics

Peer reviewing

39 manuscripts

» **Journals:** ACM Transactions on Internet of Things (TIOT), Elsevier Journal of Parallel and Distributed Computing (JPDC), IEEE Transactions on Computers (TC), IEEE Computer Architecture Letters (CAL), IEEE Micro, IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS), Wiley Interdisciplinary Reviews (WIREs): Data Mining and Knowledge Discovery

» **Conferences:** ISCA'24, ISCA'23, ICPP'22, CDC'22, ISCA'22, IPDPS' 21, CDC'20

References

Abhishek Bhattacharjee
A. Bartlett Giamatti Professor, Dept. of CS, Yale University
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Robert Bendheim and Lynn Bendheim Thoman Professor in Neuroscience, Princeton University
jdc@princeton.edu

James E. Smith
Emeritus Professor, University of Wisconsin-Madison
Adjunct Professor, Dept. of Electrical & Computer Engineering (ECE), CMU
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